

# **ELECTRONIC COMPUTERS WITHIN THE ORDNANCE CORPS HISTORICAL MONOGRAPH FROM 1961**

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## **PREFACE**

This historical monograph covers the pioneer efforts and subsequent contributions of the U.S. Army Ordnance Corps in the field of automatic electronic computing systems during the period 1942 through 1961.

No comprehensive history of electronic computers within the U.S. Army Ordnance Corps had previously been compiled and for this reason the sources for this monograph were many and varied. In general, however, these sources consisted of books (i.e., open literature), computer manuals, reports, interviews, and data prepared especially for this monograph by personnel of the Computing Laboratory, Ballistic Research Laboratory, Aberdeen Proving Ground, MD.

Mr. Martin H. Weik, Technical Staff Assistant, Computing Laboratory, BRL, assisted the author during the entire course of preparation of the monograph and supplied much of the information used in its compilation. Mr. Weik also prepared The Computer Tree which is included in Chapter VII.

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## **INTRODUCTION**

It is quite well known that the United States Army Ordnance Corps has made many significant contributions to both science and industry. Of all its contributions however, few can match the importance of the Ordnance Corps' pioneer efforts in the field of electronic computers. In the interest of national defense, the development of electronic computing systems could not wait until normal economic laws brought about the supply of systems through commercial demand. Therefore, recognizing the urgent need for such computers, the Ordnance Corps initiated the development work and supplied the funds that led to the first high-speed, electronic, automatic computer. This computer, called the ENIAC (Electronic Numerical Integrator And Computer), was proposed in 1942 and completed in 1946.

The installation of the ENIAC in 1947 in the Ballistic Research Laboratory at Aberdeen Proving Ground, MD, marked the beginning of the widespread use of electronic computing machines. Since the advent of the ENIAC, a large expansion has taken place in the computer field. Investment rates in computing equipment in the United States rose from ten million dollars per year in 1953 to one hundred million dollars per year in 1956. Present (1961) expenditures for computing equipment has passed the billion dollars per year mark.

Electronic computers find wide use throughout the Department of Defense and many other government agencies. Almost every commodity industry such as oil, steel, and rubber is utilizing computing equipment for both scientific and commercial applications. Service industries, such as banking, transportation, and insurance have applied large scale computing systems toward the solution of problems in the fields of accounting, reservations control, and bookkeeping. Manufacturers have used computing systems for design engineering and scientific research. Many systems are being utilized for inventory and stock control. The determination of manufacturing plant location and stock parts storage are being made by linear programming methods. Electronic computers are used by the construction industry for design and location of structures and road nets. Many digital computers form a part of closed loop industrial process control systems. Where the processing of large quantities of data are necessary, computing systems are invaluable.

It must be left for the historian of the future to accurately evaluate the effect of automatic computing machines on man's destiny. It is yet too early to make even a good guess. However, one thing is certain: electronic computers have ushered in a change equal to that of the Industrial Revolution. By the harnessing of mechanical power (steam engine, etc.) man was able to perform work beyond the

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capacity of his own muscles (or that of beasts of burden) and his world changed as a result. He could travel at speeds undreamed of in earlier times, he could fabricate structures never before possible, and he could build machinery to perform intricate work and produce large quantities of consumer goods at low cost. By the development of machinery for handling information and thus enabling decisions to be made automatically by mechanizing the logic of mental process, man is now able to perform mental work beyond the capacity of his brain. Many problems that have remained unsolved for years because the calculations were too formidable for a human to perform can now be handled by electronic computers. Aircraft design, ballistic crystallography, electron optics, astronomy, pure mathematics, and weather forecasting are just a few of the activities in which automatic computing machines are and will continue to play ever increasingly important roles.

At this point it might be well to consider the question: "What is an automatic computer?" An automatic computer is a machine so constructed that it can perform a complicated sequence of arithmetical and logical operations at high speeds, without human intervention or assistance. The present-day automatic computers utilize electronic circuits as the major operating components and are capable of computing speeds of the order of a few millimicroseconds per logical decision. We can properly refer to this class of machines as high-speed electronic automatic computers.

It is the term "automatic," however, that designates the most important characteristic of the modern electronic computer. This is its ability to guide and control itself during the course of its data processing action. The human operator is needed only to set up and start the machine, which can then operate without human intervention, guidance, or direction. However, the machine is self-directing only within definite prescribed limits which must be predetermined by the operator during the setup of the machine and during programming.

Automatic computers perform many operations which previously were done only by human labor and this has led some writers to refer to automatic computers as "giant brains." They definitely are not electronic brains and do not "think" in the creative sense of the word. A human mind must first determine a way of solving the problem and then instruct the computer how to solve the problem when given the data. The human operation of preparing the instructions for the automatic computer is called programming, and the resulting set of instructions is called a program or a routine. Without a program, an automatic computer cannot perform any data processing.

All computers, whether mechanical or electronic, can be divided into two distinct classes, depending on the form in which information is handled. If the information is handled in the form of letters or digits they are classed as digital computers. If the information is handled in the form of an electrical equivalent of physical variables, they are classed as analog computers. Analog computers may also represent numerical quantities by such physical variables as translation, rotation, voltage, or resistance. The slide rule and the anti-aircraft predictor are examples of analog computers. The digital computer utilizes numbers in a given scale of notation to represent all the quantities that occur in a problem or a calculation. The abacus and the desk calculator are examples of digital computers.

In a very general way it can be said that the advantages of the digital computer compared to the analog computer, are its greater flexibility and greater precision, while its disadvantages are its higher cost and greater complexity.

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More and more emphasis is being placed on the digital computer although there are still some applications where the analog computer is desirable. Throughout the Ordnance Corps the digital computer is the one most widely used for the various Ordnance applications. The analog computer finds use primarily in the older antiaircraft and antimissile fire control devices.

The importance of automatic computers to the U.S. Army Ordnance Corps is well illustrated by the extensive use of various types of computers at Ordnance Corps installations. An inventory of computers within the Ordnance Corps for the Fiscal Year 1961 lists a total of 112 computers of 36 different types in use at 26 Ordnance Corps installations. (See Appendix V).

At Aberdeen Proving Ground, for example, the Computing Laboratory has a personnel strength representing 12% of the total personnel of the Ballistic Research Laboratory. The Computing Laboratory employs 122 persons. These include: 51 Mathematicians; 15 Electronics Engineers; 4 Tabulating Equipment Operators; 38 Maintenance and Supporting personnel; and 14 military.

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## **CHAPTER I -- PRE-ELECTRONIC COMPUTING DEVICES**

The first high-speed electronic automatic computer, the ENIAC, was put into operation at Aberdeen Proving Ground in 1947 and introduced an era of possibilities never before available to the field of computation. It was one of the most significant developments of our time because it enabled us to expand our knowledge in almost every field through limitless quantities of accurate, inexpensive computation performed at high speeds.

Prior to the advent of the ENIAC, however, were thousands of years of development to produce devices which could remove the drudgery of computation. The very first requirement was the invention of a means to record numbers. Various means were used in early times to do this. The Hebrews, Greeks, and Romans, for example, used the letters of their alphabets to represent numbers, but these systems did not lend themselves to easy computation of mathematical problems. Anyone familiar with the Roman numeral system can imagine the difficulty in multiplying CCXVII by XXIX to get MMMMMMCCXCIII.

In spite of clumsy systems of recording numbers Egyptians, Greeks and Romans were nonetheless able to perform computations. A method of finger computation evolved and at some time prior to 600 B.C. an ingenious calculating device, the abacus, was developed and used by them. This calculating device employed a place system and was built around the base ten. Strangely enough it seems never to have occurred to those people to write numerals in this same system. That idea was to come many years later from India.

The Roman-type abacus found its way to the Orient around the twelfth century A.D. and today it still remains the principal means of computing in China and Japan. It is a simple device and a skilled operator can add, subtract, multiply, and divide with amazing speed. In fact, the champion abacus operator of Japan some years ago defeated a man using an electric calculating machine. The

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achievement of such speed and accuracy on the abacus, however, requires considerable training, which is one disadvantage of the abacus.

The modern abacus consists of a rectangular frame with a number of rods or wires. These rods are divided into two unequal portions by a transverse bar. On the upper, smaller portion of each rod are two beads and on the lower portion five beads. (The modern Japanese abacus has one bead above and four beads below the bar.) The whole acts as a numerical register, each rod representing a decimal order as in our familiar "arabic" notation.

The chief disadvantage of the abacus is that the operator must perform his calculations mentally. The device merely stores his results step by step. It does not perform the actual calculations as does the modern desk calculator.

As mentioned previously, in spite of the use of the abacus by the Greeks and Romans the Western peoples did not develop a convenient system of numeration. This was accomplished by Hindu scholars nearly two thousand years ago. They developed the symbols and the place system which enables us to express any number, no matter how large or small it may be. This system is easy to learn and simple to use. It is built around the base ten, although any number might have been used. It is possible that the base of ten was selected because man had always used his fingers for counting.

The Hindu numerals with their place system were carried westward by merchants and scholars and finally reached Spain in the tenth century. However, it was not until the fifteenth century that they finally prevailed in the Western World and took their present form 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9. This development opened the door to modern mathematics. Around 1600 John Napier, a Scottish mathematician, invented logarithms and also prepared a convenient multiplication table on pieces of wood or bone. "Napier's bones," as they were called, had no practical value but his logarithms did. Around 1632 William Oughtred in England made the first slide rule by inscribing logarithms on wood or ivory. The slide rule is an analog computer which is still widely used by scientists and engineers throughout the entire world.

Shortly after Napier's achievements, around 1642, Blaise Pascal in France constructed an adding machine that resembled the modern desk calculator. This machine consisted of a series of ratchet-driven wheels with the numbers 0 to 9 on them. Although it was a simple device and could only add and subtract it embodied one very important development which is an essential part of the digital computing technique, namely a means of making the "carry over" into an automatic process. It also indicated the possibility of multiplying numbers by successive addition. For the first time a machine was built that approached automatic computing because it removed a function from the operator to the machine.

In 1671 Gottfried Leibnitz, in Germany, invented the stepped wheel, a cylindrical drum having nine teeth of increasing length along its surface. When the drum was rotated, a gear sliding on an axis parallel to that of the drum engaged some of the teeth, thereby undergoing a corresponding number of rotation steps. The Leibnitz wheel made it possible to multiply quickly by repeated additions. From then onwards a variety of improved calculating machines were devised, all based on the original idea of wheels moved around in steps, and by the nineteenth century commercial models began to appear. The Thomas machine (France) embodied this principle and, starting in 1822, was the first to be

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manufactured for widespread use. It was a dependable, crank-operated, four-process machine. In 1885 Burroughs, in the United States, produced an adding machine and in 1902 the first machine with completely automatic multiplication and division was built by Rechner, also in the United States. Several machines were designed in various countries and by 1920, with the fully automatic Monroe machine, we reach the stage of desk calculators familiar to us in banks, offices, and laboratories. These are the machines that do most of the world's computation, the modern ones being electrically driven and assuming more and more of the operator's functions.

These machines, however, are limited in scope and require the constant attention of a human operator to supply them with numbers and to record on paper the result of each stage of the calculation before proceeding to the next one. They do save time and mental effort but they are not fast enough where very large quantities of numerical data have to be handled. It must also be noted that they are not true forerunners of the modern electronic computers.

The principles of modern computers, albeit in mechanical form, were laid down by Charles Babbage in England. Starting in 1812 he attempted to build an automatic mechanical calculator. He was familiar with Muller's idea for a difference engine (1786) and Jaques' idea for controlling a loom by means of punched holes (1775). He incorporated both ideas and actually made models of a difference engine which was card controlled. Technical problems of construction were too great for mechanical engineering of that period and the computer was never finished. Later, Babbage conceived an even more ambitious idea. He worked on the design of an analytical engine, which, had it been built, would have incorporated ideas familiar to the modern digital computer.

Babbage's new idea was to extend the capabilities of the difference engine so that it could not merely add and print, but also multiply, divide, and call for new data from its human operator. In order for the analytical engine to perform the tasks expected of it, it was necessary to express all the possible instructions to the machine in the form of stereotyped commands. Such a procedure is known as the logic or the logical design of a computer, and Babbage's engine was strikingly modern in regard to its logical design. Except for the need of a human attendant to read into the machine values from mathematical tables, this engine was logically parallel to most of the recent automatic computers. Naturally the speed of computation would have been far below that of the modern calculator (it could perform one addition per second), since Babbage had to use the purely mechanical techniques available in his day.

A significant part of his design for an analytical engine was the use of a "store" for holding the partial results of arithmetic operations performed in what he called the "mill." To feed numbers into the machine he proposed a system using patterns of holes punched in cards, while the results of calculations were to be presented by a mechanism which would set up the appropriate numerals in type ready for printing. Another proposal was that the engine should be capable of deciding on a course of action in the light of partial results obtained. He called this the "control." All these ideas have become features of the modern digital computer, and it is mainly because of them that our present-day machines are so fast in operation and so versatile in their range of calculations.

The next important development along this line was made by Hollerith and Powers during 1880 - 1890. Working for the United States Census Bureau they required some means of handling large

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masses of information. This led to the development of the first key punch, the first sorter, and the first tabulator, all using large punched cards. The patterns of round holes in the cards were formed by using a crude hand-punching device. The cards could be sorted into the series or order wanted, and then tabulated to reduce the census data to manageable form. Hollerith did not use the punched cards to control the course of computation, but simply used the holes in the cards to carry information. Hollerith and Powers also employed the electromagnetic techniques in their machine, that is, information on the card (hole or no hole) was converted into electric impulses, and the electric impulses actuated devices known as relays.

In 1925, at the Massachusetts Institute of Technology, Dr. Vannevar Bush and his associates began studying the problem of designing a machine to solve differential equations. In 1927, Dr. Bush started work on a mechanical differential analyzer. He experimented with mechanisms that would integrate, add, multiply, etc., and methods of connecting them together in a machine. Originally he made use of electrical currents flowing through watt-hour meters, which integrate the electrical power absorbed by circuits attached to them. Later he reverted to the mechanical integrators of the wheel and disc type. A major part of the success of the machine depended on a device whereby a very small turning force would do a rather large amount of work. By careful design of the discs and of the wheel mountings, Dr. Bush was able to make the integrators accurate, and, by introducing torque amplifiers to take the loads off the wheels so that they rotated very freely, he was able to reduce the slippage between the wheel and the disc. He combined a frame with the integrators, which contained movable shafts, changeable gears and couplings, input hand-wheels and output recording pens for producing a readable result.

By 1930 the first differential analyzer was finished. It was entirely mechanical, having no electrical parts except the motors. Its disadvantage was the great deal of work required in changing from one problem to another. This involved undoing old mechanical connections between shafts and setting up new ones. For this reason the design of a second analyzer was begun in 1935, on which all connections could be made electrically.

As early as 1932 personnel of the Ballistic Section at Aberdeen Proving Ground had investigated the possible use of the Differential Analyzer for ballistic computations. The machine was used to compute numerous trajectories including a set sufficient for the preparation of a complete range table. It was also tested on interior ballistic problems. A careful study and evaluation of the results of this investigation led to the following conclusions:

1. Such a machine could be built at Aberdeen Proving Ground.
2. The machine could perform various kinds of ballistic computations with the necessary accuracy.
3. Operation and maintenance would require no unusual skill.
4. The speed of the machine was such that it would insure greatly increased output of work by the Ballistic Section in any emergency.
5. It could perform routine work at a smaller total expenditure of funds.

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6. Its use in the preparation of range tables would replace numerous complicated and indirect methods by simple, uniform and direct process.

7. Its use would permit the investigation of various problems, the solution of which was necessary to any advance in ballistic theory or practice but which previously could not be studied because existing methods required a prohibitive amount of computing labor.

It was decided to use the Bush Differential Analyzer at Aberdeen Proving Ground and its installation was completed in 1935. After final adjustment and trials it was used in the computation of two firing tables. These were completed with gratifying results by mid 1936.

The Bush Differential Analyzer, an analog device, was installed under the direction of Major James Guion, who was in charge of the Ballistic Computing Section at Aberdeen Proving Ground at that time. Major Guion had been quick to realize the value of this continuous variable calculator to the computational needs of the Ordnance Department. The availability of this machine and the experience that was gained in its use were invaluable to the Ordnance Department during the crucial transition period prior to America's entry into World War II.

The analyzer installed at APG had ten integrating units and provisions for two input and two output tables. However, despite its value as an important mechanical aid to computation it had certain limitations. The torque amplifier, for example, although simple in mechanical design, frequently failed toward the end of a long trajectory run with the loss of the preceding computation and an appreciable delay associated with its repair. This type of failure and the interference that it caused with the carrying out of computations at the Ballistic Research Laboratory led to extensive study to overcome this problem.

At the outbreak of World War II in Europe the officer in charge of ballistic computations at APG was Lt. P. N. Gillon. He immediately recognized the immensity of the task that would fall upon the Ordnance Department in the event of United States participation in the war and this prompted him to seek both marked improvement in mechanical aids to computation and augmented facilities for its accomplishment. A number of very important things were undertaken to accomplish this purpose.

The Moore School of Electrical Engineering of the University of Pennsylvania had a Bush Differential Analyzer of somewhat larger capacity than the one at Aberdeen Proving Ground. It had fourteen integrating units instead of ten. Therefore the Ordnance Department awarded a contract to the University of Pennsylvania for the utilization of this device. Several additional contracts were later awarded to the University to carry out different phases of the increasingly important role which it was to play in the computation activities of the Ordnance Department during the war.

Lt. P. N. Gillon, in his capacity as officer in charge of ballistic computations, conferred frequently with Dean Pender, Professor Brainerd, and their associates at the Moore School in order to effect proper coordination of the computational work at the two localities, Philadelphia and Aberdeen. There was a very talented group at the Moore School under the direction of Professor Brainerd and as a result of Lt. Gillon's discussions with them Assistant Professor Weygand undertook to develop an electronic torque amplifier to replace the mechanical torque amplifiers on the Bush Differential Analyzers. This work was eminently successful and, in addition, photoelectric followers were developed by the Moore

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School group for both the input and output tables of the analyzer. As a result of these accomplishments the productive capacity of the analyzers at both the Moore School and Aberdeen Proving Ground were enhanced by at least an order of magnitude.

During World War II the Bush Differential Analyzer was used primarily to compute trajectories for firing tables and to prepare trajectory charts for use with VT fuzes. The machine could compute a 60-second trajectory in about 15 minutes, whereas a human operator using a desk calculator required about 20 hours to perform the same computation. Its value to the Ordnance Department during the war years was tremendous.

The next major development, prior to the advent of the high-speed electronic automatic computer, came in 1944 when Howard Aiken, in cooperation with some IBM engineers and some graduate students at Harvard University, completed the Mark I Relay Computer, also called the Automatic Sequence- Controlled Calculator.

This machine performed thousands of calculating steps, one after another, according to a scheme fixed ahead of time. Its individual operations were automatic, once the punched tape fixing the chain of operations had been put on the machine, and it was sequence-controlled, since control over the sequence of its operations was built into the machine.

The principle of operation of the Mark I Relay Computer was electro- mechanical. It combined the two applications of the concept of state, that is, the information for processing was represented by patterns of open and closed relays (like the patterns of holes and no holes which Babbage used).

Although the machine was efficient, fast, and capable of solving a variety of problems its speed could not approach that of the electronic computer, which is the next state in the development of computers and the subject of this monograph. Nevertheless, it holds a permanent place in the history of development of calculating machines, since it was the first automatic machine to be completed.

(BRL at APG used two types of relay computers during 1947-1954. Two IBM Relay Calculators were used for a short time but were not successful. Two Bell Relay Computers were used. They were accurate, but slow and required expert maintenance. Dust and humidity adversely affected their operation. However, many useful results were obtained from the twin Bell Relay Computers during many years of successful operation. One good feature of the Bell Relay Machines was that they would run 16 hours overnight, unattended. A problem regularly would be placed on the computer at 4:00 PM. The next morning, arriving operating personnel would find the problem solved and the machine waiting, or the machine still feverishly running the problem to a successful conclusion. Many times, if it was felt that the machines would complete a problem during the night, a new problem was set before the machine for it to tackle until personnel arrived the next morning. This mode of operation increased the productivity of the computers with a minimum of personnel. Of course, once in a while a dirty relay would cause a stoppage, for the Bell A and the Bell B would either run without error or not run at all.)

## **CHAPTER II -- ENIAC**

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## **The World's First Electronic Automatic Computer**

When the United States entered World War II the Ordnance Department was faced with a task of gigantic proportions.

(The Ordnance Department was renamed Ordnance Corps in 1950.)

It was responsible for design, procurement, distribution, and maintenance of ordnance materiel for the Army Ground Forces, the Army Air Force, and, in some categories the Navy. This task immediately engendered an accelerated research and development program. Of extreme importance in this program was the preparation of firing and bombing tables. This work was conducted at the Ballistic Research Laboratory at Aberdeen Proving Ground, MD, where the experimental data necessary to the computation of such tables was also obtained. When it is realized that for each weapon-ammunition combination the preparation of a separate firing table is required, the magnitude of the computations involving an entirely new series of weapons is easily seen.

The preparation of firing and bombing tables was performed by the Ballistic Computing Section of the Ballistic Research Laboratory. This section was composed at that time of a few civilian employees who were trained and highly skilled in the conventional methods of computation. In addition to desk calculators the group had available the Bush Differential Analyzer, which was capable of handling many types of problems but also had certain limitations. Captain P. N. Gillon, who was in charge of ballistic computations at the laboratory, recognized the need for improved aids to computation to cope with the greatly expanding computational activities.

Early in 1942 additional personnel, including military, were acquired to work in the Ballistic Computing Section at Aberdeen Proving Ground. Despite this increase in personnel work began to pile up and in June 1942 a contract was made with the Moore School of Electrical Engineering of the University of Pennsylvania to operate its Bush Differential Analyzer exclusively for the Army. In September 1942 the Chief of Ordnance granted permission to operate a computing branch at the Moore School as a substation of Aberdeen Proving Ground. In this way the Ordnance Department could meet its requirements in computing. The two analyzers were operated day and night during the war.

The group at the Moore School of Electrical Engineering was supervised by Lt. Herman Goldstine, a member of the Aberdeen staff, who was assigned there at Captain Gillon's request to head the computational and training activities. Lt. Goldstine was especially well qualified for this assignment because of his outstanding mathematical ability and his understanding and appreciation of Ordnance problems in the field of ballistic computation

(Lt. H. Goldstine had received his doctorate in mathematics at the University of Chicago).

Early in 1943, Captain Goldstine (promoted in the interim) and Professor Brainerd brought to Lt. Colonel Gillon (promoted 1942) the outline of the technical concepts underlying the design of an electronic computer. The idea had been conceived by Dr. J. Mauchly in 1942 as a result of work he had done previously with problems in weather study and physics that required great masses of numerical information to be handled, and also as a result of his experience at the Moore School of Electrical Engineering in the calculation of trajectories. This outline was prepared at Captain Goldstine's request by Dr. Mauchly and Mr. J. P. Eckert, Jr. Lt. Colonel Gillon, who meanwhile had been assigned to the Office, Chief of Ordnance as Deputy Chief of the Service Branch of the Technical Division, realized

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fully that formidable opposition would be offered to the initiation and prosecution of a development of this sort, especially in view of the highly speculative character of its successful completion. However, he also fully realized that there existed an urgent need for some means to perform computing at high speeds, not only for ballistic computations but also for the research activities of the Ordnance Department. Therefore he undertook to obtain the necessary authorization for its initiation and assumed full responsibility for its support and supervision.

It was Colonel L. Simon, Lt. Colonel P. N. Gillon, Captain H. Goldstine, and Mr. S. Feltman who secured the support of the Ordnance Department and continually stimulated the Moore School of Electrical Engineering of the University of Pennsylvania to further their efforts with respect to aids to computation. Dr. J. Mauchly, Mr. J. P. Eckert, Jr., Professor G. Brainerd, Dr. H. Pender and other members of the University of Pennsylvania staff applied their abilities to the problem of designing an electronic automatic computer. The result was a proposal, which was submitted to the Chief of Ordnance on 8 April 1943.

The original agreement between the United States of America and the trustees of the University of Pennsylvania, dated 5 June 1943, called for six months of "research and development of an electronic numerical integrator and computer and delivery of a report thereon." (The initial letters of the words describing the device were used to form its name - ENIAC.) This initial contract, R.A.D. 1078-W-670-ORD-4926 committed \$61,700 in Ordnance Department funds under appropriation number ORD 61166 P610-07-A1005-23. Nine supplements to this contract extended the work to 1946, increased the amount ultimately to a total of \$486,804.22, assigned technical supervision to the Ballistic Research Laboratory at Aberdeen Proving Ground, and called for the delivery of a working "pilot model," first to be operable at the University of Pennsylvania and then to be delivered to the BRL at APG.

From this point forward, the research staff and faculty of the Moore School of Electrical Engineering under Dr. H. Pender undertook energetic prosecution of the development pursuant to the terms of the Ordnance contract. The project was placed under the supervision of Professor Brainerd, with Mr. J. P. Eckert, Jr., as chief engineer, and Dr. J. Mauchly who provided the original outline for this development, as principal consultant. The resident supervisor for the Ordnance Department, Captain H. Goldstine, not only exercised extraordinary detailed and highly competent supervision for the Army but also contributed greatly to the mathematical side of the undertaking. As in all important undertakings which achieve important results, this was a work of many individuals.

Many meetings and conferences were held during the early days of development of the electronic numerical integrator and computer (ENIAC). Naturally many technical decisions had to be made. Then, as now, universities had an insatiable appetite for research, but in this case it was essential that the Ordnance Department obtain an operating device within a reasonable period of time. For example, there was always the temptation to increase the capability of the ENIAC, hence, when mercury delay lines came up for consideration as internal memory, Lt. Colonel Gillon, as the responsible supervisor for the Ordnance Department, insisted on the tried and tested decade ring counters in spite of the inherently reduced storage capacity.

(However, in view of the great promise of the mercury delay lines he obtained authorization for a new and separate contract calling for a new machine, using these delay lines. This machine, when completed, was the EDVAC and will be discussed in the next chapter.)

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In this way precious time for the development of the ENIAC was not lost. The ENIAC was constructed at the Moore School component by component, beginning with the cycling unit and an accumulator in June 1944. This was followed in rapid succession by the initiating unit and function tables in September 1945, and the divider and square-root unit in October 1945. Final assembly took place during the fall of 1945 and the ENIAC was formally dedicated at the Moore School of Electrical Engineering of the University of Pennsylvania on 15 February 1946. Acceptance by the Ordnance Department took place in July 1946.

Four years had elapsed since the original suggestion by Dr. John W. Mauchly that an all-electronic computer be built which could rapidly perform the vast amount of calculations required for the solution of the many complex problems facing the Ordnance Department. All through 1946 the ENIAC remained at the Moore School, working out numerical solutions to problems in such fields as atomic energy and ballistic trajectories.

In the winter of 1946-1947 the ENIAC was dismantled at the Moore School of Electrical Engineering and the first units arrived at Aberdeen Proving Ground, MD, in January 1947. By August of 1947 the ENIAC became operational again. It was the world's first electronic automatic computer and it not only opened up greater possibilities for advances in science and engineering but also started a new multi-billion dollar industry.

War circumstances had made it imperative to construct the ENIAC out of conventional electronic circuits and elements with a minimum of redesign. This fact, together with the requirements for capacity, speed, and accuracy, led to an extremely large machine. Its 30 separate units, plus power supply and forced air cooling, weighed over thirty tons and occupied 1,800 square feet. Its 19,000 vacuum tubes (16 different types), 1,500 relays, and many thousands of resistors, capacitors, and inductors consumed about 174 kilowatts of electrical power.

The main part of ENIAC consisted of 42 panels arranged around three sides of a room. Each panel was about 9 feet high, 2 feet wide, and 1 foot thick. Air ducts at the top of all the panels were provided for drawing off the hot air around the tubes. There were also 5 portable panels which could be rolled from place to place.

ENIAC was the prototype from which most other modern computers evolved. It embodied almost all of the components and concepts of later high-speed, storage and control devices. The counters and accumulators of the machine, with more sophisticated innovations, were made up of combinations of these basic elements.

The various units were interconnected through two sets of coaxial lines carried in "trays" running around the length of the machine. One set was called digit trays and was used for carrying pulse groups representing numerical data from one unit to another. The other set was called program trays and carried pulses controlling the sequence of operations of the different units and could be plugged into the trays in accordance with the set-up for any particular computation.

The machine worked with numbers expressed in the decimal system and could handle numbers of ten digits. The decimal system was chosen, in spite of advantages of other systems, because of the familiarity of its use.

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The ENIAC could discriminate the sign of a number, compare quantities for equality, add, subtract, multiply, divide, and extract square roots. A maximum of twenty 10-digit decimal numbers could be stored. The accumulators combined the functions of an adding machine and storage unit. No central memory unit existed, storage being localized within the functioning units of the computer.

The primary aim of the designers was to achieve speed by making ENIAC as all-electronic as possible. The only mechanical elements in the final product were actually external to the calculator itself. These were an International Business Machines (IBM) Corporation card reader for input, and IBM card punch for output, and the 1,500 associated relays. Another design objective was to make the electronics simple and reliable. This goal was achieved by utilizing vacuum tubes in a minimum of basic circuit combinations. To ensure reliable operation, circuits were constructed of rigidly tested standard components, which were operated at current, voltage, and power levels below their normal ratings. Accuracy of computation was assured by designing the basic circuits to work independently of the variable tolerances of their components. Numbers were not represented by electrical quantities which could be affected by changes in tolerance, but only by the presence or absence of dynamic pulses. Pulse groups representing the digits of a single number were transmitted simultaneously on different lines, requiring eleven lines in each digit tray for the ten decimal digits and the sign.

The gate, a circuit which would produce an output dependent upon a specified input, performed the switching or logical AND function.

(AND is a term peculiar to computer engineering. It is a mathematical operator used to denote a process of logic whereby a statement is true if and only if all input conditions are met or are true.) It consisted of a single pentode which had a control voltage applied to its suppressor grid. Its function was similar to that of a single pole switch in that it "opened" (i.e., passed a pulse pattern) when the suppressor grid was positive and "closed" when the suppressor grid was negative.

The buffer, an isolating circuit used to avoid any reaction of a driven circuit upon the corresponding driving circuit, contained two or more tubes connected through a common load resistor to form a circuit with the logical properties of the word OR.

(OR is a term peculiar to computer engineering. It is a mathematical operator used to denote a process of logic whereby a statement is true if at least one of the input conditions is met or is true.)

The grids of the tubes were normally biased at the cut-off point so that a positive input to any tube in the combination produced a negative output.

The flip-flop circuit contained two triodes so connected that only one would conduct at a given time. The bi-stable device had two inputs and two outputs. In the SET, or normal position, one side of the output was positive, the other negative. In the RESET or abnormal position, these polarities were reversed. Logically, the flip-flop performed the functions of memory and that of a double pole, double throw switch. The state of each flip-flop was indicated by a neon lamp on the front panel of the computer units.

A group of ten flip-flops, (0-9), interconnected to count digit pulses, formed a decade ring counter which was capable of adding and storing numbers. The counter possessed the following characteristics:

1. At any one time only one flip-flop could be in the RESET state.

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2. A pulse to the counter input reset the initial flip-flop in the chain.
3. The circuit could be cleared so that a specific flip-flop was in the RESET position while the others remained in the SET position.

Each flip-flop of a counter was termed a stage, and reception of a pulse at the input side advanced the counter by one stage. Information recirculated through the counter; i.e., the last stage was coupled to the first. A variation of the basic counter circuit, the PM (plus or minus) counter, controlled the sign of a number in the accumulator.

Ten decade ring counters, one per decimal place, plus one PM counter, formed the basic arithmetic and storage unit of ENIAC, and was called the accumulator. The decade ring counters were equipped with ten transmission circuits so that when any ring passed the nine positions, a pulse was passed to the next ring in the series. Input pulses reaching the accumulator added to or subtracted from its contents.

The accumulator was an essential element in all of ENIAC's arithmetic operations. Addition required two accumulators, one transferring its contents to the other. Subtraction, accomplished by a complement-and-add process, also used two accumulators. In normal multiplication four accumulators stored the multiplier and multiplicand and accumulated the partial products. In division they shifted the remainder and stored the numerator, denominator, and quotient. The function table utilized the accumulators for storage of the argument and accumulation of the function value.

ENIAC was a synchronous system, operating under the control of pulses from a cycling unit. The pulses were emitted a 10-microsecond intervals. The over-all timing cycle or repetition rate was 200 microseconds, which was the time required for one addition. Pulses were transmitted to all units continuously and simultaneously, and each computer operation took an integral number of addition times. For checking and trouble-shooting purposes, the cycling unit circuitry included provisions for operation in a one-addition or one-pulse-at-a-time mode.

The ENIAC was not originally designed as an internally-programmed computer. The program was set up manually by varying switches and cable connections. However, means for altering the program and repeating its iterative steps were built into the master programmer. Digit trays, which were long racks of co-axial cables, carried the data from one functioning unit to another. Program trays transferred instructions (i.e., programs) in a similar manner. In purely repetitive calculations, the basic computing sequence was set by hand. The master programmer automatically controlled repetition and changed the sequence as required.

The master programmer contained ten six-stage counters, each routing incoming program pulses over a field of six output channels. The position of the counters was controlled by either the number of pulses which had been supplied to the output channels or by the number of pulses received at a special input terminal. In this fashion the number of sequences could be fixed in advance or made contingent on the results of a computation.

Each functioning unit of ENIAC was equipped with local program control circuits. These circuits contained switches which were set for the function required. When the local program circuit was stimulated by a program pulse, the unit performed the desired operation. After this was completed a

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program completion pulse was emitted, via the program tray coaxial line, to the next unit in the operational sequence.

In addition to its cycling unit, twenty accumulators, and master programmer, ENIAC included an initiating unit, a high-speed multiplier, a divider, a square-root unit, and three portable function tables.

The initiating unit turned ENIAC on and off, cleared it, and initiated computation.

The high-speed multiplier did its work in much the same fashion as a human would. It contained a built-in multiplication table capable of multiplying up to 9 times 9. Multiplication of the multiplicand by each digit of the multiplier took one addition time. The left and right hand figures of each product of a digit of the multiplicand and the multiplier were accumulated separately to form two partial products, which when combined, formed the final product. The multiplication process for two 10-digit numbers took 2.6 milliseconds.

The divider and square-root unit worked by repeated subtraction and addition, a time-consuming procedure which took an average of 25 milliseconds for a 10-digit number. The divisor was subtracted from the dividend, and the sign of the partial remainder was tested after each step. When the sign became negative, the remainder was shifted up-scale and the divisor was added until the sum became positive. An accumulator serving as a quotient register kept a count of the numbers of additions and subtractions for the successive decimal places. Extraction of square root was a similar process.

The principal purpose of the function tables, which actually were banks of switch-controlled resistor matrices, was the storage of the arbitrary functions called for by the problem. The switches selected one of 12 digits and two signs for each of the 104 values of an independent variable that were stored in each table. The functional similarity between later computers and the ENIAC is rather astounding when one considers the time difference in their development.

The ENIAC was built primarily for integration of the equations of external ballistics by a step-by-step process, but it was flexible enough to be applied to a wide range of large-scale computations other than numerical integration of differential equations.

There were three ways of supplying the machine with information (numbers or instructions). Numbers could be put into the machine by means of punch cards fed into the Card Reader, panel 46, or by means of switches on the Constant Transmitter, panels 37 to 39. Numbers or instructions could also be put into the ENIAC by means of the Function Tables, panels 43 to 45, where there were dial switches which were set by hand. Instructions could also go into the machine by setting the switches, and by plugging the inputs and outputs etc., of the wires or lines along which numbers and instructions traveled.

Information came out of the machine in two ways. Numbers came out punched on cards by the Summary Punch, panel 47. They were then printed in another room by means of a separate IBM tabulator. Numbers could also be read out of the machine by means of the lights in the neon bulbs mounted on each accumulator. These could be read when the panel was not computing.

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In applying the ENIAC to a particular computation it was first necessary to break down the work into a number of basic computing sequences, the ordering of which was controlled by the master programmer. Next, each sequence was broken down into the individual computing operations of which it was composed. These were then carried out through the interconnections of the arithmetical units of the machine.

In programming calculations other than for trajectories (for which the machine was primarily designed) the chief drawback was the small memory capacity into which numbers could be recorded and from which they could be read automatically. This memory capacity consisted of the twenty accumulators, but four of these were used for multiplication and four for division. Therefore no more than sixteen, and often fewer, would be available for storing intermediate results. This capacity was adequate for the original purpose of the machine but where other types of computations were involved their method of calculation was determined by this memory capacity.

The machine had an indefinitely large memory capacity in the form of punched cards, but recording into and reading from this memory was slow. Also, the attention of an operator was required in some cases to transfer cards from the punch to the reader. The increased range of the machine was thus obtained at the expense of speed and the fully automatic character of its operation.

The first few years of use of the ENIAC at Aberdeen Proving Ground were difficult ones for the operating and maintenance crews. The computer represented the largest collection of interconnected electronic circuitry then in existence, and its thousands of components had to remain operational simultaneously. The result was a huge preventive maintenance and testing program, which finally led to some major modifications of the system.

Operating experience with the ENIAC indicated that 90% of the service interruptions were caused by vacuum tube failures. At the beginning of 1950 a tube surveillance program was initiated whereby tubes were life-tested and statistical data on the failures were compiled. All this led to methods of tube testing which were unique at the time. The information gained, on the other hand, led to many improvements in vacuum tubes themselves. Procurement of large quantities of improved, reliable tubes, however, became a difficult problem because conventional tubes were not ideal for use in computers.

An additional problem involving vacuum tubes was that of dissipating the heat. This was a problem of major proportions and was never solved for the ENIAC. Special air conditioning had not been provided and the blower system was not adequate to dissipate the heat into the warm, humid atmosphere. The result was a shortening of tube life which caused long periods of inoperation. For example, the checking routine alone took about eight hours. Eventually modifications to the machine were made which eliminated about 3,000 tubes.

As previously mentioned ENIAC originally had not been designed as an internally stored fixed program computer. Programming new problems meant weeks of checking and set up time, since the ENIAC was designed as a general- purpose computer with logical changes provided by plug-and-socket connections between accumulators, function tables, and input-output units. However, the ENIAC's primary area of application was ballistics, mainly the differential equations of motion. In view of this, the ENIAC was converted into an internally stored fixed-program computer when Dr.

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John von Neumann of the Institute for Advanced Study at Princeton suggested that code selection be made by means of switches so that cable connections could remain fixed for most standard trajectory problems. After that improvement considerable time was saved when problems were changed.

The ENIAC performed arithmetic and transfer operations simultaneously. Concurrent operation caused programming difficulties. A converter code was devised to permit serial operation. Each function table, as a result of these changes, became available for the storage of 600 two-decimal digit instructions.

These revolutionary modifications, which were installed early in 1948 converted ENIAC into a serial instruction execution machine with internal parallel transfer of decimal information. The original plugable connections came to be regarded as permanent wiring by most BRL personnel.

By 1950 it was realized that the commercial source of electrical power utilized by ENIAC was too unstable for reliable operation. Fluctuations in voltage caused errors to occur in the machine and also loss of information. Since the ENIAC was operating on a 24-hour per day basis such interruptions were extremely undesirable.

The problem was finally solved by installing a motor generator as a source of power for the machine. The motor was supplied by the power line and in turn drove the generator which supplied the load to ENIAC. The inertia of the motor took care of fluctuations in power line voltage and kept the power to ENIAC constant.

In 1951 the converter code was revised by the addition of a faster- access function table which increased the stored program capacity of the ENIAC. Previously all switches had to be set by hand. The new unit utilized plugboards which could be pre-wired and simply plugged in. This reduced set up time for each new problem, increased the memory, and speeded operations.

By July 1953 the final improvement had been made on the ENIAC. This was the Static Magnetic Memory installed by the Burroughs Corporation of Philadelphia, PA. By mid 1951 the engineers at BRL had realized the necessity of increasing the internal memory capacity of the ENIAC. Aside from the twenty high-speed storage registers in the machine, all other storage came from present switches or punched cards. The switches could not be modified during the program and consumed considerable time for their initial setting. The punched cards were unduly slow for use as a high-speed internal memory medium.

The Burroughs Corporation had been investigating the techniques of using magnetic cores for circuits and storage elements and had demonstrated them. Because of the experience gained in these investigations the Burroughs Corporation was awarded the contract to design the Static Magnetic Memory for the ENIAC. It was to consist of 100 words of first access time storage.

An important consideration in the design of the Magnetic Memory system was the characteristics of the magnetic material used. The techniques for reproducing high-quality magnetic cores had not been fully perfected and so the Memory System was designed to operate reliably with the quality of cores available in quantity production.

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The design of the Memory System itself had to take into consideration the characteristics already built into the ENIAC. They were not particularly adaptable to the new techniques that had been built up since the development and design of the ENIAC. The language problem was of paramount importance. The ENIAC used a pulse-count code so that, to represent a single decimal digit, ten signals were applied to a single wire. Therefore, to store 100 words of 10 decimal digits, plus its sign, 9,100 bits of storage would be required. Economy dictated that code converters should be used to translate the pulse-count code of the ENIAC to a four-bit binary expression to represent a single decimal digit. This code conversion reduced the number of storage bits from 9,100 to 4,100.

The address selection in the ENIAC was of a decimal code to select one of the 100 words of storage in the memory.

The problem was to develop a storage system, controlled by ENIAC, so that any one of the 100 words could be selected to store or to extract information on the command of ENIAC, and take less than one addition cycle. The memory was to contain its own power supply and necessary cooling ducts. Emphasis was to be placed on reliability and accessibility to all electronic and magnetic parts.

The unit was designed and constructed by the Burroughs Corporation and installed for use. The interconnection between the Memory and ENIAC was through 48 lines. In addition to these signal lines, provisions were made for single-phase and three-phase power to the Memory.

During the period 1946 - 1955 the ENIAC was operated successfully for a total of 80,223 hours of operation. It performed about five thousand arithmetic operations for each second of its useful life. ENIAC led the computer field through 1952 when it served as the main computation machine for the solution of the scientific problems of the nation. It surpassed all other existing computers in solving problems involving a large number of arithmetic operations. It was the major instrument for the computation of all ballistic tables for the U.S. Army and Air Force. In addition to ballistics, the ENIAC's field of application included weather prediction, atomic energy calculations, cosmic ray studies, thermal ignition, random number studies, wind tunnel design, and other scientific uses.

EDVAC and ORDVAC (subjects of following chapters) both faster than ENIAC, began to share the Computing Laboratory's workload with the ENIAC in 1953. It became apparent almost immediately that the ENIAC would have to be modified if it were to remain competitive, economical, and efficient. Modifications were therefore made on the ENIAC. In addition to the modifications previously mentioned there was a high-speed electronic shifter, which reduced by 80% the time required for numerical shifting and eliminated numerous tubes and program units. It was installed early in 1952.

In spite of modernization, however, and the fact that trouble-free operating time remained at about 100 hours per week, operating costs were far above those of the other machines. The workload was gradually shifted to these other machines and at 11:45 PM on 2 October 1955 the power to ENIAC was removed. The rapid progress of computer technology, spurred by the ENIAC itself, had made the device obsolete.

## **CHAPTER III -- EDVAC**

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During the course of design and construction of the ENIAC it was necessary to freeze its engineering design very early in order to meet the urgent need for an operational computer. However, as the construction proceeded it became increasingly obvious that it was both possible and desirable to design a computer which would be much smaller in size than the ENIAC and yet have greater flexibility and better mathematical performance. This conclusion was reached as a result of consideration of the computing speed possible with electronic design, the operating characteristics of the circuit elements required in electronic computers, and the nature of the mathematical problems which can be solved economically only by large scale, high-speed computers. The Ballistic Research Laboratory at Aberdeen Proving Ground, MD, became interested in this possibility and in late 1944 it was agreed that, as work on the ENIAC permitted, the design and construction of such a machine should be undertaken by the Moore School of Electrical Engineering under the sponsorship of the Office, Chief of Ordnance, U.S. Army.

The problem of computer design had attracted the attention of one of the world's leading mathematicians, Dr. John von Neumann, who was the author of a report published on 30 June 1945 by the Moore School of Electrical Engineering, University of Pennsylvania. This report, prepared under the Ordnance Department contract for ENIAC, contained a specific proposal for the design of "a very high-speed automatic digital computing system, and in particular with its logical control".

(Quote from Dr. von Neumann's report entitled, "First Draft of a Report on the EDVAC.")

Dr. von Neumann defined an automatic computing system as "a device which can carry out instructions to perform calculations of a considerable order of complexity." He then stated that instructions governing this operation must be given to the device in absolutely exhaustive detail; that instructions must be given in some form the device can sense; and that once these instructions are given to the device it must be able to carry them out completely and without any need for further intelligent human intervention.

In analyzing the contemplated device Dr. von Neumann made five distinctions:

1. Since the device is primarily a computer it will have to perform the elementary operations of arithmetic most frequently. Therefore, it should contain specialized organs for just these operations, i.e., addition, subtraction, multiplication, and division.
2. The logical control of the device (i.e., proper sequencing of its operations) can best be carried out by a central control organ.
3. A device which is to carry out long and complicated sequences of operation must have a considerable memory capacity.
4. The device must have organs to transfer information from the outside recording medium of the device into the central arithmetic part and central control part, and the memory. These organs form its input.
5. The device must have organs to transfer information from the central arithmetic part and central control part, and the memory into the outside recording medium. These organs form its output.

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The group at the University of Pennsylvania was reconstituted to include Dr. John von Neumann, Dr. A. W. Burks, and Captain H. Goldstine, as well as Mr. J. Eckert, and Dr. J. Mauchly. Their efforts eventually resulted in the design and construction of a computer along the lines suggested by Dr. von Neumann. A progress report on this machine was published by the Moore School of Electrical Engineering in September 1945. It covered a number of possible physical designs, all of which would meet the general logical requirements. This was followed early in 1946 by a conference attended by Dean Harold Pender and Dr. Irven Travis of the Moore School, Colonel Paul Gillon of OCO, and Dr. John von Neumann of the Institute for Advanced Study. It was decided at this conference that experience with a pilot model of the new calculator was urgently needed in order to obtain information about coding problems and operating characteristics, which could then be applied to the design of a very comprehensive calculating machine. It therefore seemed expedient that the Moore School of Electrical Engineering, University of Pennsylvania, should immediately proceed with the design and construction of a small preliminary model for the Ballistic Research Laboratory, while the Institute for Advanced Study, Princeton, should undertake a study program leading to the establishment of design requirements for a large-scale comprehensive computer.

On 12 April 1946 Contract W-36-034-ORD-7593 was signed between the Ordnance Department and the Trustees of the University of Pennsylvania to prepare a preliminary model of the machine. The original amount of money allotted was \$100,000.00 and the final cost, after fifteen supplements to the basic contract, was \$467,000.00. The basic contract stipulated that, "the Contractor shall, as an independent Contractor and not as an agent of the Government, design and develop a preliminary model of a small Electronic Discrete Variable Automatic Calculator

(The word calculator was used in the contract although the word computer is more generally used.) (hereinafter referred to as "EDVAC") that will demonstrate the feasibility of producing subsequently an EDVAC having comprehensive properties envisioned in the report entitled "Automatic High-Speed Computing, University of Pennsylvania," prepared by the Contractor under its contract No. W-670-ORD-4926, and shall construct and deliver to the Government f.o.b., Philadelphia, PA, on or before 30 June 1947, one (1) preliminary model of said EDVAC.

In working out the preliminary designs for this small EDVAC, Moore School personnel worked in close cooperation with representatives of the Ballistic Research Laboratory who were then operating the ENIAC. Both the Moore School and BRL personnel very naturally desired this small EDVAC to be as comprehensive as possible and still meet the requirements for small size and simplicity. In order to obtain a mutually agreeable interpretation of the term "Small Preliminary Model of EDVAC," a conference was held at Aberdeen Proving Ground on 9 October 1946, attended by Dean Pender and Dr. Travis of the Moore School, Colonel G. F. Powell, and Mr. S. Feltman of OCO, Colonel L. E. Simon of BRL, Dr. von Neumann of IAS, Mr. H. Diamond of the National Bureau of Standards, and other representatives of these activities.

The Moore School of Electrical Engineering presented three possible designs, briefly described as follows:

EDVAC I. A very simple binary computer, with automatic addition, subtraction, and multiplication, programmed division, and no internal checking. Memory capacity of 1,000 words.

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EDVAC II. A simple binary coded decimal computer, with fixed decimal point, all four basic arithmetic processes automatic, and automatic checking in the computer. Memory capacity of 1,000 words.

EDVAC III. A more comprehensive machine, with automatic floating decimal point, and all the automatic features listed under EDVAC II. Memory capacity of 4,000 words.

It was decided in this conference that a binary machine based on the EDVAC I design, but with automatic division and automatic checking, was desirable.

(A binary machine is one that uses the binary system of notation. This system employs only two digits, 0 and 1, in contrast to the decimal system which employs ten digits, 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9. The binary system is useful in automatic computers not only because of the two-state system of an electronic device (i.e., current on or off), but also because the circuits required to do arithmetic are not too difficult to design and react rapidly, hence arithmetic operations can be performed at high rates. Counting in the binary system is done by twos instead of by tens as in the decimal system. For example the binary number 1011 signifies: 1 eight, plus 0 fours, plus 1 two, plus 1 one which is eleven and expressed as 11 in the decimal system.)

This machine was designated as the EDVAC 1.5. It was also decided that the National Bureau of Standards would design and supply the equipment for preparing and printing from the magnetic wire used in the Reader-Recorder of the EDVAC.

As the design of the EDVAC 1.5 progressed, further discussions with BRL representatives indicated the desirability of introducing certain additional orders, such as the "Extract" order, into the coding scheme. Since these changes, together with another change necessary to give increased stability of the memory, would have considerably increased the complexity of the EDVAC, another conference was held at Aberdeen Proving Ground on 27 May 1947, in which two alternative proposals were considered. These were EDVAC 1.5A and EDVAC 1.5B, with and without the added coding flexibility respectively. No final decision was reached at this conference, and Dr. R. F. Clippinger of the Ballistic Research Laboratory at APG was appointed to consider the various possibilities and submit a report. As a result of this report the EDVAC 1.5B design was approved with minor modification.

The major features of this computer were the use of the binary system of numeration, the serial arithmetic mode, the four-address command structure, and duplicate circuitry for check purposes. This computer dropped the use of the train of pulses to represent decimal digits in favor of the binary system, which was much better suited to the two-stateness of the electronic circuits. The design features of EDVAC served as a model for many later computers.

EDVAC was the first internally stored program computer to be built, a major improvement over the ENIAC. One of the major disadvantages of the ENIAC had been the fact that it required considerable human effort to change to different programs. ENIAC was programmed by setting switches on function tables and by changing the wiring (wired programs).

The EDVAC was to be organized essentially as follows:

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1. Reader-Recorder. This unit would contain the three wire drives, associated servo-mechanisms, amplifiers for the magnetic reading, recording and erasing heads, and the equipment required to transfer information from the heads to the processing delay and vice versa.

2. Control. This unit would contain all operating buttons, indicating lamps, control switches, and an oscilloscope for aid in maintenance. The control sends special orders, set up on switches, to the dispatcher in order to start the machine, and may send words, set up on another set of switches, to the high-speed memory.

(The Reader-Recorder and the control are the only units containing devices to be manipulated by the operator.)

3. Dispatcher. This unit would decode orders received from the control and memory. It would also emit control signals to the other units, which need them to perform their functions. Its electrical delay memory would retain the order while it is being performed.

4. High-Speed Memory. This would consist of two identical units, each containing 64 acoustic delay lines and associated regeneration circuits. Each line or "tank" would have a capacity of 8 words. Each memory cabinet would also house three short tanks of one word capacity, which would be used by the algebraic units. These tanks are used for temporary storage of the operands during arithmetic operations. The cabinets would contain, in addition, apparatus to decode the addresses received from the dispatcher and select the memory position whose contents are to be transferred out of the memory or to be replaced by incoming data.

5. Computer. This unit would perform the rational operations (addition, subtraction, multiplication, and division) on pairs of numbers with signs received from the high-speed memory, and return the result to the memory at the appropriate time. The arithmetic unit would be in duplicate and the answers compared, digit for digit. Any disagreement would stop the machine and give an "abnormal halt" indication.

6. Timer. This would emit clock pulses at intervals of 1 microsecond, and timing pulses at intervals of 48 microseconds.

The National Bureau of Standards undertook to construct an input-output system for the EDVAC. It consisted of modified teletype equipment for inscribing key-boarded information to the magnetic wires, and for outscribing information from the magnetic wires to automatically typewritten characters on rolls of ordinary paper.

After briefly covering the organization of EDVAC, the report then dealt with design problems. These were of utmost importance in order that all requirements could be met.

As mentioned previously, EDVAC was required to be much smaller than the ENIAC and to have greater flexibility and better mathematical performance. It was assumed that its speed would be at least equal to that of the ENIAC. Reliability was an obvious requirement and previous operating experience with various computers indicated the need for emphasis on design to achieve maximum reliability. Also needed was an adequate checking system.

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In order to obtain high overall speed in the solution of complex mathematical problems, high functional speed had to be supplemented by an adequately large high-speed memory. In late 1946 a mercury acoustic delay memory had been built by the Moore School of Electrical Engineering. This device had operated stably and reliably for long periods. Although other types of memory gave promise of eventually becoming useful, it did not appear, at that time, that any other type could become available for immediate use. Therefore, the mercury memory was selected for EDVAC.

The next question to be considered was the capacity of the memory. In discussions of possible problems for digital computers, requirements for a high-speed memory of as many as 10,000 words were encountered.

(A "word" is, in computing language, a combination of digits handled as a unit by the machine.) However, many problems could be handled with a memory of 1,000 words or less. It was shown that a mercury acoustic memory of 1,024 words would require nearly the same amount of equipment as the rest of the computer. A reduction in size to 512 words would result in a saving of only 25% in size and cost, and would slow down the solution of many problems. On the other hand, an increase to 2,048 words would increase the size and cost by 50%, while this additional capacity would be required only by a relatively small number of problems. Therefore, a high-speed memory capacity of 1,024 was selected as the best compromise between the mathematical requirement and the requirement that EDVAC should be much smaller than ENIAC.

In the construction of the memory device liquid delay lines were used since this was a straightforward way to avoid interference from transverse waves. Quartz transducers were used because of their stability and low cost and because X-cut quartz crystals were well suited to the production of compressional waves in the liquid. Of a large number of liquids considered, mercury was found to give the best acoustic match with the quartz crystals and for this reason it was used.

There were some disadvantages with mercury, however. It was dense and expensive and it was contaminated by most metals. Contamination in the EDVAC was completely eliminated by the use of glass tubes with tungsten electrodes. Weight and cost were reduced by use of tubes of the smallest diameter consistent with good performance.

The temperature of the mercury tanks was stabilized by enclosing the tanks in heavy extruded U-sections of Dow metal clamped to thick vertical plates of the same material, mounted back to back with heating elements between them. The temperature control system was designed to maintain the temperature well within the desired limits. Thirty-two long tanks were mounted on each plate. The entire assembly was enclosed in a heat insulating case and a pair of coaxial leads was brought out from each tank to its associated recirculating chassis. This chassis was mounted outside the insulating case where it was cooled by circulation of the ventilating air. Two of these assemblies, mounted in separate cabinets, were constructed for the EDVAC.

Some consideration was given to the possibility of using a temperature compensating device with each tank, instead of the system for controlling the temperature of the assembly. This idea was attractive in many ways but would have required considerable development. It would also have had the disadvantage of requiring 128 individual controls, as compared to the two controls required for the

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two-bank stabilized system which was actually used. In the former case the failure of any one of the 128 controls could incapacitate the system.

As previously indicated, functional operation had to be fast enough to give operational speeds comparable with the ENIAC, in spite of the fact that the serial operation of the EDVAC would be inherently slower than the parallel operation of the ENIAC. An upper limit to the operational speed was set by the pulse repetition frequency. The frequency selected, one megacycle per second, was determined primarily by the characteristics of the commercially available vacuum tubes used in the machine.

In all of the circuit design, emphasis was placed on reliability, simplicity, economy of vacuum tubes, and, to the limited extent practicable, standardization of circuits. Two circuits were built into plug-in units for ease and speed in maintenance. These were the flip-flop and the mercury memory circulating units. Crystal gating circuits were extensively used to decrease the number of tubes required. All available information indicated that the life of the germanium crystals, at the voltages and currents used in the EDVAC, would be many times that of the tubes they replaced.

(Experience with the ENIAC had demonstrated that for long life and reliable operation, tubes should not be operated at average currents or dissipations above half of the values for which they are normally rated.)

Since the field of electronic digital computer design was new as the EDVAC was being developed, it was impossible to set up hard and fast rules of circuit design. Such guiding principles as were established were subject to modification as additional information became available. Nevertheless, certain guiding principles in circuit design were established and adhered to where possible.

A number of methods for checking the algebraic operations were considered, and, taking into account the maintenance problem, it was concluded that the most satisfactory method was to build two identical algebraic units, carry out all algebraic operations in both units simultaneously, and compare results at five points. Other checks were provided in the order type selector and dispatcher for detecting forbidden orders, pulses in switching blanks, and other coding and functional errors.

The problem of driving pulse lines received a great deal of attention. The method used in the ENIAC (driving of lines by means of cathode followers in parallel) was unsuitable for use in the EDVAC because of the large number of tubes required to drive certain heavily loaded lines. Two new methods were devised. The first consisted of blocking oscillators for low duty cycle lines and the second of a power pulse transformer driven by tube banks for high duty cycle lines. These systems would require only about one sixth as many tubes as the earlier circuits.

The use of magnetic wire as input and output medium for the EDVAC was given consideration; however, the scheme never culminated in an operating wire unit.

The EDVAC was housed in steel cabinets 86 inches high. In all except the memory units, the chassis are mounted vertically, with doors front and back for ready access to both sides of each chassis. This arrangement simplified maintenance and was convenient for installation of the ventilating system.

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Relatively few manual controls were required, since they were used only for starting and stopping the machine, examining the progress of a calculation, modifying a routine, or checking functional operation.

The input-output system was the result of collaboration between the National Bureau of Standards, the Institute for Advanced Study, and the Moore School of Electrical Engineering. It was designed by the Bureau of Standards and utilized, insofar as possible, standard commercial equipment in its construction, particularly teletype equipment and standard wire recording components.

The system was divided into two parts, the inscriber and the outscriber. The inscriber was used to translate the information prepared by the programmer into a code on the magnetic wire which served as an input for the EDVAC. The outscriber printed the information, which the output of EDVAC had placed on a magnetic wire, on paper for human use.

Two teletype keyboarding machines were used in the inscriber. The first was called the preliminary perforator and was used to prepare a preliminary "chadless" paper tape by typing the programmer's instructions. Chadless tape was used in order that the character might be printed over the perforations to assist in checking. This preliminary tape was fed into a solenoid-operated tape reader, the output of which was fed through the verifier to the perforator-printer, which would retype the same code. The output of this machine would then be fed back to the verifier. If the character agrees with the character on the tape it is punched on the verified tape, and the tape reader advances the preliminary tape to the next character. If the two characters disagree, an indicator lamp lights on the verifier panel and the perforator-printer locks until the source of disagreement is eliminated. Provision was also made to convert from the decimal into the binary notation.

As work under the contract progressed, it became necessary from time to time to freeze logical planning and design characteristics in order that the project should result in the completion of the EDVAC. If this were not done the result would merely have been the establishment of the specifications and techniques then representative of the existing state of the art. Certain design characteristics of the completed machine represented the state of the art two years previous, others of one year previous, while some were current characteristics. As often happens in development projects of this nature, the freezing of design occurred later than had been anticipated, partly because early design decisions had been unsound and partly because it is never possible to prevent research-minded personnel from continuing to incorporate desirable improvements which result in a better instrument but are accompanied by a later completion date. In the case of EDVAC a delay of about one year occurred, but the machine possessed a capability far beyond that envisioned in the preliminary report or in the contract and its supplements.

The EDVAC was constructed at the Moore School of Electrical Engineering and delivered to the BRL Computing Laboratory at Aberdeen Proving Ground in August 1949 for installation. After the installation was completed there were two major engineering jobs to be done before EDVAC could become operational. These were:

1. The memory recirculate amplifiers had to be redesigned to provide additional loop gain.

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2. Input-output equipment had to be designed, constructed and installed to provide a means of getting data into and out of the machine.

Although there were very few logical errors in the EDVAC in the initial design, it had more than its share of marginal circuits which had to be modified before it could become operational. These problems were solved in approximately eighteen months and the machine started to operate on a limited basis late in 1951. By early 1952 it was averaging 15-20 hours of useful time per week for solving mathematical problems. By 1961 EDVAC was operating 145 hours out of a 168-hour week.

After the EDVAC was installed at APG there were three major engineering problems to be solved.

The first problem was to redesign the mercury memory amplifier to get better gain bandwidth product and to get better long-term stability.

The second problem was to go through every circuit of the machine to eliminate marginal circuits. Many hours were required to redesign the gating and pulse amplifier circuits.

The third problem was to design an input-output system for the EDVAC. This resulted in the construction of a shift register for assembling asynchronous data from a paper tape reader, which was installed as part of the machine. Controls were installed on other equipment for printing data from the EDVAC onto paper tape and to employ a teletype writer.

Over the past ten years several pieces of new equipment have been added to the EDVAC to increase its flexibility and capabilities to solve problems.

These were:

1. The IBM card input-output adapter unit, which was installed in June 1953.
2. A magnetic drum which was installed in the latter part of 1954. It provided an additional 4,608 words of medium-speed storage.
3. A built-in Floating Point Arithmetic Unit, which was added early in 1958. This unit increased the operation speed of EDVAC by a factor of 12 when working with floating point numbers.
4. A magnetic tape system which was added in late 1960 for additional storage.

The application of EDVAC at the Ballistic Research Laboratory is as follows:

1. Exterior ballistics problems such as high altitude, solar and lunar trajectories, computation for the preparation of firing tables, and guidance control data for Ordnance weapons, including free-flight and guided missiles.
2. Interior ballistics problems, including projectile, propellant and launcher behavior, e.g., physical characteristics of solid propellants, equilibrium composition and thermodynamic properties of rocket propellants, computation of detonation waves for reflected shock waves, vibration of gun barrels and the flow of fluids in porous media.

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3. Terminal ballistics problems, including nuclear, fragmentation, and penetration effects in such areas as explosion kinetics, shaped charge behavior, ignition, and heat transfer.
4. Ballistic measurement problems, including photogrammetric, ionospheric, and damping of satellite spin calculations, reduction of satellite doppler tracking data, and computation of satellite orbital elements.
5. Weapon systems evaluation problems, including anti-aircraft and anti-missile evaluation, war game problems, linear programming for solution of Army logistical problems, probabilities of mine detonations, and lethal area and kill probabilities of mine detonations, and lethal area and kill probability studies of missiles.

The following paragraphs present a general description of the way in which EDVAC works. As already mentioned EDVAC is a synchronous automatically-sequenced serial binary electronic digital computer. The word serial refers to the storage device wherein the digits of a stored number become available one at a time.

(In a parallel system all the digits of a number become available simultaneously.)

The machine has a high-speed memory of 1,024 words and a medium-speed memory of 4,608 words.

A word, in the strictly electronic part of the EDVAC, consists of a sequence of 44 binary characters or digits followed by 4 blanks. A pulse signifies 1 and the absence of a pulse signifies 0. The pulse positions are spaced at intervals of one microsecond and are about 0.3 microseconds in duration. A complete word thus requires 48 microseconds to pass a given point, and this interval of time is known as a minor cycle.

The high-speed memory consists of mercury delay lines with regenerating amplifiers. The lines are known as long tanks and each tank stores eight words. A long tank is 384 microseconds in time length and this interval is known as a major cycle. Eight minor cycles are required for the contents of a long tank to pass a given point in the circuit. The entire memory consists of 128 long tanks.

In the case of a number the first binary character which emerges will represent the sign (the presence of a pulse denotes "minus"), the next is the least significant digit, and the last is the most significant digit. The characters are arranged so that increasing time corresponds to the direction right to left in written notation. The decimal point in a number is normally interpreted to be at the extreme left, since the multiplication and division operations were designed in such a way as to make this the simplest interpretation.

If the word represents an instruction, the first four digits (in time) determine what the instruction is, that is, whether the operation to be performed is addition, subtraction, multiplication etc., while the remaining forty digits represent four "addresses" in the high-speed memory. Ten binary characters are necessary and sufficient to specify a position in the high-speed memory.

The EDVAC is a 4-address machine and the four addresses are used to specify the locations of the numbers to be operated upon, where to store the results of the operation, and where to find the next instruction in the sequence of operations.

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The EDVAC memory system consists of 128 long tanks, 6 short tanks, associated amplifiers and control equipment. The circuits are so arranged that a word may be handled as follows: 1. Read into a given memory position.

2. Allowed to circulate.

3. Withdrawn from a memory and restored by means of an external path.

4. Withdrawn and not restored.

The memory system is divided into two banks, left and right, each containing its own heater and controls. The mercury tank heaters are split into two sections, an upper and a lower section. Each section is controlled by a thermostat to hold the temperature at 50 degree Celsius plus or minus 1/4 degree Celsius.

The average operating time per instruction for EDVAC is as follows:

1. Addition 864 microseconds

2. Subtraction 864 microseconds

3. Compare 696 microseconds

4. Extract 696 microseconds

5. Multiply and round off 2,880 microseconds

6. Divide and round off 2,928 microseconds

7. Multiply exact 2,928 microseconds

8. Divide exact 2,928 microseconds

9. Floating point add 960 microseconds

10. Floating point subtract 960 microseconds

11. Floating point multiply 1,248 microseconds

12. Floating point divide 2,352 microseconds

Normal operation of the EDVAC proceeds in the following manner. The operator will take a program deck of IBM cards and load these into the IBM card reader. A special order to read the IBM cards will then be set up on the control switches. Another switch is set to direct the control to read this special order. The initiate button is then depressed, causing the special order to be sent to the dispatchers where it is acted upon and the information on the cards is read into the high-speed memory. The switch is then set to a continuous mode. The machine starts and continues to operate until a programmed halt is reached. Audible and visual signals inform the operator all-well during a run and audible and visual

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signals are given when the machine ceases computing. The operator then removes the cards which have recorded the results. The cards are placed in a tabulator which prints the results.

An examination of one type of problem solved by EDVAC, the preparation of a firing table, will give some idea of the capability of this computer. The basic problem in the preparation of a firing table is that of computing the trajectory of a projectile by solving a system of differential equations. This system of equations is dependent on the weapon system under consideration, and often, as in the case of a rocket during its powered flight, must be complex enough to account for the fact that the projectile is a rigid body acted on by several forces and moments.

In the past, the equations of motion were solved by numerical integration using a desk calculating machine. For the preparation of a firing table, therefore, a relatively small number of trajectories was computed at finite intervals of some parameters and intermediate values were obtained by interpolation over rather large intervals.

With the advent of the high-speed computers came the possibility of computing as many trajectories as desired and, consequently, of providing firing tables limited in detail only by the desires of the using combat arm or technical service. It is interesting to note that the computation of a trajectory for a conventional artillery projectile was done in the past with a desk calculator in about four hours and that the same computation would require about 30 seconds on either the ENIAC or EDVAC and about 10 seconds on the ORDVAC. Furthermore, and of greater importance, it was now possible to escape the necessity of using many of the approximations that were used in the past. For example, the EDVAC can solve the complex system of equations for a rocket during powered flight in about 3 minutes for each second of flight time. In the past this problem was treated by using some gross approximations which resulted in poor descriptions of the rocket flight.

The introduction of high-speed computers has increased the accuracy and volume of computational capabilities to the level that is required to support the firing table mission, a level that is almost beyond comprehension on the basis of its being done by desk calculators.

EDVAC operates on a 24-hour daily schedule, 7 days per week. A series of tests are run at the start of each 8-hour shift to check the machine and its auxiliary equipment. Approximately 12 hours per week are spent in testing the EDVAC for proper operation and checking out improvements, and the remaining time is used for code checking and problem solving.

The EDVAC operating efficiency has steadily increased over the past several years. The average running time per week during 1960 was 145 hours. Over a period of nine years EDVAC increased its efficiency from 15-20 hours to 145 hours per week. By 1961 it appeared, however, that its operating efficiency had almost reached its maximum.

By the end of 1961 EDVAC was still in operation and was expected to continue operating for at least one year after the BRLESC would begin full operation.

(BRLESC, the first electronic computer fully designed and developed by the BRL, was expected to be operational by late 1961.)

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After ten years of operation EDVAC was still in use because of its great reliability and productivity, its low operating cost, its high operating efficiency, and its speed and flexibility in solving certain types of problems required by the Ballistic Research Laboratory. (See Appendix II for technical data of EDVAC.)

## **CHAPTER IV -- ORDVAC**

ORDVAC (Ordnance Variable Automatic Computer) belongs to the group of computers whose basic logic was developed by the Institute for Advanced Study at Princeton, NJ and utilized in a prototype computer developed at the Institute. This ORDVAC family of computers includes such machines as the ILLIAC, ORACLE, AVIDAC, MANIAC, JOHNNIAC, MISTIC, and CYCLONE.

(ILLIAC - Illinois Automatic Computer; ORACLE - Oak Ridge Automatic Computer and Logical Engine; AVIDAC - Argonne Version of the Institute's Digital Automatic Computer; MANIAC - Mathematical Analyzer Numerical Integrator and Computer; JOHNNIAC - John (v. Neumann) Integrator and Automatic Computer; MISTIC - Michigan State Digital Computer; CYCLONE - (an arbitrary name indicating high speed) Iowa State U.)

ORDVAC was constructed by the University of Illinois for the Ballistic Research Laboratory at Aberdeen Proving Ground, under a contract from the Ordnance Department. The contract number was, W11-022-ORD-11362--RAD ORDTB 9-10675--ORD PROJ TB3-0007J--negotiated under ASPR 3-205. The contracting agency was the Chicago Ordnance District and the period of the contract was 15 April 1949 to 31 October 1951.

Through arrangements made by Dean L. N. Ridenour, the University of Illinois began construction of ORDVAC about 15 April 1949. The efforts of many individuals went into the construction of the machine. The University of Illinois received the cooperation of members of the staff of the Ballistic Research Laboratory in the procurement of materials and the assignment of members of the staff of BRL during the final phases of construction. These BRL staff members were: Dr. P. M. Kintner, Mr. G. H. Leichner, and Mr. C. R. Williams. In addition, Dr. L. A. Delsasso and Dr. R. F. Clippinger followed the work from its inception.

The logical structure of ORDVAC was patterned after a machine described in the 28 June 1946 report, "Preliminary Consideration of the Logical Design of an Electronic Computing Instrument" by Burks, Goldstine and von Neumann of the Institute for Advanced Study. The University of Illinois received helpful information and suggestions arising from discussions with Mr. J. H. Bigelow, Captain H. H. Goldstine and Mr. J. H. Pomerene of the Institute for Advanced Study, especially during the early period of construction of the ORDVAC. Also, drawings pertaining to the arithmetic unit and memory of the machine at the Institute for Advanced Study were furnished to the University of Illinois and some parts of these drawings, such as the registers, were copied for the ORDVAC.

It was first planned to build ORDVAC from circuit drawings obtained from the Institute for Advanced Study, but this intention was later changed and most of ORDVAC was constructed from circuits designed at the University of Illinois. The fundamental flipflop, gating and cathode follower circuits, as employed at the Institute for Advanced Study, were used however. The registers, complement gate

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and clear drivers were copied from the machine developed at the Institute for Advanced Study and the teletype units were of the kind developed at the National Bureau of Standards for the Institute for Advanced Study. Except for these, however, responsibility for the design of ORDVAC rested with the University of Illinois.

ORDVAC was provisionally accepted by the Ballistic Research Laboratory on the basis of tests conducted between 15-25 November 1951 at the University of Illinois. The machine was dismantled beginning 11 February 1952 and shipped to the BRL on 16 February 1952. During 5-6 March 1952 it successfully performed the three final acceptance tests. These were: (a) the operation of the "final test" routine for twenty hours with one error; (b) the operation of a memory "read-around" test routine requiring that the memory could be consulted ten times at each of its addresses without causing a failure at any other address (this was repeated five times); and (c) the operation of a memory flaw test for thirty minutes without an indication of a failure.

The machine was moved to the Ballistic Research Laboratory under contract: DA-11-022-ORD-680; SUB-RAD 52-56; ORDTB 2-1002; project TB3-0007. The cost of the basic system was approximately \$600,000.

The work at the University of Illinois was administered chiefly by an executive committee of the Computer Sub-committee of the University Research Board. This committee consisted of Professor N. M. Newmark, Professor A. H. Taub, Professor R. E. Meagher and Professor J. P. Nash.

The machine was designed to solve the following types of problems:

1. Exterior ballistics problems such as high altitudes, solar and lunar trajectories, computation for the preparation of firing tables and guidance control data for Ordnance weapons, including free flight and guided missiles.
2. Interior ballistic problems, including projectile, propellant and launcher behavior, e.g., physical characteristics of solid propellants, equilibrium composition and thermodynamic properties of rocket propellants, computation of detonation waves for reflected shock waves, vibration of gun barrels and the flow of fluids in porous media.
3. Terminal ballistic problems, including nuclear, fragmentation and penetration effects in such areas as explosion kinetics, shaped charge behavior, ignition, and heat transfer.
4. Ballistic measurement problems such as photogrammetric, ionospheric, and damping of satellite spin calculations, reduction of satellite doppler tracking data, and computation of satellite orbital elements.
5. Weapons systems evaluation problems, such as anti-aircraft and antimissile evaluation, war game problems, linear programming for solution of Army logistical problems, probabilities of mine detonations, and lethal area and kill probabilities of mine detonations, and lethal area and kill probability studies of missiles.

ORDVAC is a general purpose computer capable of carrying out individual arithmetic operations at high speed. It operates in the binary number system in a parallel asynchronous manner, and originally

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used an electrostatic memory. Data was originally put into the machine by punched teletype tape, later by punched cards. Data is obtained from the machine on punched cards, a teletype page printer, or punched teletype tape.

The part of ORDVAC capable of carrying out arithmetic operations on numbers supplied to it is called the arithmetic unit. It consists of three registers (two of them double registers), which are essentially storage units for holding the operands involved in arithmetic operations, a parallel 40- binary digit adder, and other subsidiary units such as the complement gate which provides the complement of the number is one of the registers.

The registers of the arithmetic unit correspond to the keyboard and dials on the common desk calculator. They hold the operands while the operations of arithmetic take place, and they present the results of these operations. The basic components of the registers are the flipflop and the gate.

ORDVAC is a parallel machine, that is, operations are performed simultaneously on all the digits of an instruction or information word. For example, when a 40-digit number is transferred from the memory into a register of the arithmetic unit, all digits are transferred simultaneously. Similarly, when a number in R3 (one of the registers) is added to a number in the accumulator, the steps in this process are carried out on all the digits at the same time.

Although ORDVAC may use several number systems, the basic one is the binary or base-two system. This system is convenient because it requires only the two digits 0 and 1 for number representation and therefore flipflops or any other two-state devices can be efficiently used. Moreover, the logical structure of the machine is based upon a two-state logic (where all decisions are of the yes-no type), so that an over-all consistency is obtained.

Many operational economies can be realized with the binary system, and the disadvantages inherent in an unfamiliar system can be overcome by requiring the machine to make all of the necessary conversions to and from more familiar systems, such as the decimal system.

The ORDVAC's new arithmetic unit has a fixed point number system and handles numbers in the range -1 to +1. It can be programmed for any number system, but the fixed point system requires a simpler control. The choice of the range -1 to +1 is dictated by the fact that the product of two numbers in this range is likewise in range.

The new arithmetic unit has an add time of 14 microseconds, a multiply time of 700 microseconds, and a divide time of 700 microseconds. All of the arithmetic operations of ORDVAC are automatic in the sense that a single order is required for each one and the sequencing is then automatically programmed.

One of the principal components of any automatic computing machine is the control. The ORDVAC control consists of some 500 vacuum tubes located in thirty chassis. Most of these chassis are quite well localized, but a few, notably those associated with the end connections, are scattered through the arithmetic unit.

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It is the function of the control to carry out the individual operations necessary for executing the orders which the programmer has combined into a routine for solving a problem. Because some of the orders require complicated sequencing and because there is a considerable variety of orders, the control is a highly interconnected component with very little duplication of circuits. These circuits are primarily combinations of four kinds of logical elements:

1. The flipflop.
2. The "and" circuit.
3. The "or" circuit.
4. The "not" circuit.

The flipflop is a device which can indicate one or the other of two states and which can be changed from one state to the other. The two states can be indicated in any of a number of different ways such as, "plus" or "minus," "yes" or "no," "on" or "off." In the ORDVAC the names given to these states are "zero" and "one."

The other three logical elements perform functions which are quite well described by their names. The "and" circuit has two inputs and one output which will have a signal on it if, and only if, there is a signal on each of the inputs. The "or" circuit is similar except that there will be a signal on the output if there is a signal on either one or both of the inputs. The "not" circuit has a signal on its output if there is no signal on the input and no signal on the output if there is a signal on the input.

The state of the machine at any time may be defined by the state of the flipflops in the machine. It is the function of the control to determine the state of ORDVAC and to change this state in accordance with the instructions provided to ORDVAC via the input and the memory.

The control operates by withdrawing instructions and numbers from the memory. In general it can be said that the control alternates the process of withdrawing pairs of instructions with the process of executing them. Most of the work of the control is done between references to the memory. For example, all of the operations of arithmetic are handled by the control. Thus in multiplication, a number of steps must be carried out between the time the multiply instruction and the multiplicand come out of the memory and the time the product is put back into the memory.

The memory unit originally used in the ORDVAC was of the Williams-type, in which information is stored as a potential distribution on the phosphor surface of a cathode ray tube.

Storage of information on the phosphor must be accomplished for periods much longer than one-tenth of a second, which is the longest safe time permitted on the cathode ray tube surface. This storage is accomplished by "regeneration." In the ORDVAC memory facilities are provided so that when the memory is not in use for arithmetic operations a test is made of each spot of the memory, in order, and each spot is regenerated by appropriately turning the beam on or off so that a "fair" dot is regenerated into a "good" dash. By this scheme it is possible to hold information in the memory for indefinite periods of time.

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In order to use ORDVAC effectively in any computation its memory must be fully or partially filled before the problem begins. This is accomplished by the part of the machine called the input. It originally used teletype tape, previously prepared by an operator using tape preparation equipment. ORDVAC was capable of controlling the operation of its input in that it can determine when to read information from the tape. The input of ORDVAC was capable of filling the entire memory in 38 minutes by the relatively slow mechanical paper tape reader.

The input-output equipment consists of teletypewriter units together with those circuits of the computer used in performing the two instructions input and print.

The input instruction takes 40 binary digits from 10 successive rows of a tape that has been previously punched with 4 binary digits per row, and puts them in order in the register R1.

The print instruction prints one word on a sheet of paper as ten sexadecimal digits. These are formed by taking the 40 binary digits in register R2, four at a time, beginning with the sign digit, and printing a corresponding base 16 symbol.

Teletype tape was also punched by ORDVAC, when it was desirable to have the output on tape. The equipment used for output was, in some part, the same as that used for the input.

During the period from 10 March 1952 to 2 October 1953 ORDVAC was available for computation a total of 8,410.18 hours. The total engineering time was 4,189.17 hours, and the remaining 1,104.65 hours composed standby time. Standby time includes all the time during which no attempt is made to operate or service the machine.

During the earlier periods of operation there had been a considerable amount of standby time. The lack of sufficiently trained personnel and the lack of programs did not make it desirable to maintain the machine over the weekends. As more programs were completed, however, and the machine's load increased, it was soon learned that operating the ORDVAC without interruption reduced the number of troubles encountered on Monday morning and enabled it to be made available for use at an earlier time. By 1954 standby time averaged 13.54 hours per week.

Between March 1952 and October 1953 an average of 37.17 hours per week was spent on code checking, 38.29 hours per week on production, and 23.03 hours per week was classified as idle time. The title "idle time" was not intended to indicate that the machine was not in use during that time. It was made to continually run a test called Leap III, but was available for other use at any time. Should the Leap III routine fail, the following time was immediately classified as unscheduled engineering until the cause of the error was corrected, and the routine successfully operated for fifteen minutes.

The normal operating schedule of ORDVAC included three periods each day during which the performance of the machine was checked. The period 0800 to 1000 hours was set aside for engineering purposes. At this time small changes and improvements could be made, troubles that may have developed during the night shifts cleared, and finally the machine could be tested by various self-checking programs. Tests were again made at the conclusion of each working day and at midnight. Upon the successful conclusion of the tests the ORDVAC was released to the mathematicians who used it during the day. On the night shifts most of the production work was performed by two

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technicians per shift who were in charge of the machine. They were not expected to understand the programs that were run, but followed explicit instructions left by the mathematicians. This system worked quite well and when a coder arrived at the Laboratory in the morning he usually found that his program had been completed.

During this period (1952-1953) about thirty different problems were placed on the ORDVAC in the course of a single average week. Ballistic computations, such as firing and bombing tables and trajectories for guided missiles and rockets, formed forty percent of the work done by ORDVAC. Vulnerability computations and data reductions formed twenty-five percent and twenty percent respectively. Research problems formed ten percent and systems tests formed five percent of the work.

Three classes of tests were used to test the units of ORDVAC. A read-around-ratio test was used for checking the memory, an input-output test was used to test the teletype and card handling equipment, and the Leap III test was used to test the arithmetic and control section and to give a further check on the memory.

ORDVAC was used as much as possible to test itself by a highly repetitive use of its components. In this way marginal and intermittent errors could be detected that would otherwise not have been found. The usual memory errors were not too difficult to repair. The cause of arithmetic errors were harder to detect since their effect might propagate. Intermittent failures were especially troublesome if the error frequency was low. In this case an attempt would be made to increase the error rate by special routines which would strain the circuits to their limit, by vibrating the circuit components, by varying filament or supply voltages, or by a combination of the above.

When ORDVAC was delivered to the Ballistic Research Laboratory its input device was a standard-speed five hole teletype tape reader and its output a teletype page printer. With this equipment, the time necessary to load the entire memory of 1,024 addresses was 38 minutes. The time required to print the contents of the entire memory was the same. It was soon realized, however, that a change was necessary in the input in order to speed up the operation of the computer. Within a few weeks after ORDVAC was placed in operation a control circuit had been designed and built for a modified tape reader which allowed information to be read into the machine at five times the previous rate. The memory could now be filled in 7.5 minutes. This unit performed exceptionally well but input and output still remained the bottleneck to more efficient use of the machine.

The most important change in input-output was the addition of card handling equipment. This was desirable, especially since the ENIAC already used punched cards and such a system was soon to be developed for the EDVAC. There were two possible systems to be considered. The first was an external system in which information punched on card was to be automatically converted to its binary equivalent by external apparatus. The second was an internal conversion system based on utilizing the ORDVAC itself to accomplish the necessary transformation. The second method was chosen.

The advantages of the internal system lay in the elimination of the necessity for extensive additional equipment and the achievement of maximum reliability through the use of established machine operations. The greatest disadvantage of the internal system was that a significant portion of the memory capacity was committed to the decimal-to-binary conversion program. The space required for both input and output conversions amounted to 200 words or approximately one-fifth of the memory.

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Later improvements of the memory made it possible to further reduce the size of the program, however.

The system was based on double register gating in which the entire 80-column output could be gated to or from the ORDVAC simultaneously. An electronic control circuit, actuated by signals generated in the card punch or card reader, allowed the contents of the ORDVAC registers to be stored in the memory or changed between each row of a card.

This system proved quite reliable and was preferred over tape by the mathematicians. The usual practice was to first prepare a program on tape and immediately transcribe it to cards with a special routine that would automatically read from the tape and punch twenty-four words per card in binary form.

The electrostatic memory had always been the most troublesome unit of ORDVAC. Prior to June 1953 the memory operated rather consistently at a read-around-ratio of 10 to 16. A restriction of 10 placed on the coders resulted in slower routines or routines that occupied a larger portion of the memory. In addition to read-around-ratio-difficulties there existed the problem of obtaining cathode-ray tubes whose screens were free of impurities. Cathode-ray tubes, type 3KP1, were used for storage. Approximately 25% of those tested were acceptable, most rejections having been due to impurities which could cause improper storage. Up to May 1953 approximately sixty cathode-ray tubes had been removed from the machine for various reasons. About two-thirds of the total number were removed because of the impurities in their screens. Five were removed without proper cause, and the remaining tubes were removed because voltage adjustments would no longer hold the read-around-ratio of those tubes above 10. No cathode-ray tubes burned out under normal operating conditions, although five were deliberately burned out when subjected to abnormal conditions.

In May 1953 it was learned that the University of Illinois was obtaining improved read-around by using a three-dot system. In this system two dots represent a one and three dots represent a zero. The first and third dots occur at the same location. ORDVAC was changed from a two-dot system about 1 June 1953. Considerable difficulty was encountered with the sensing pulse, and in order to strengthen it sufficiently so that its magnitude would not vary with the number of zeros sensed, it was necessary to incorporate a pulse transformer into the circuit. The new system caused the read-around-ratio to be increased by a factor of three so that it was then varying between 32 and 48.

In an attempt to further improve the reliability of the electrostatic memory, a number of cathode-ray tubes of type C73376B, under development by RCA, were obtained and installed in the ORDVAC. By 1954 they had been in the ORDVAC for 1,500 hours and had operated satisfactorily. The read-around-ratio increased to 80 and the flaw problem no longer existed since these tubes were virtually free of flaws.

The greatest difficulty experienced with the new tubes was due to their centering characteristics. Upon installation, a large number of tubes had to be immediately removed, because extremities of the 1,024-spot raster projected beyond the useful surface of the screens. Ten tubes were removed for this reason. The ORDVAC, like most machines using electrostatic memories, operated its cathode-ray tubes in a parallel manner, so that any positioning of the raster which is beneficial to one tube might render other tubes completely useless.

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A test was made on the centering of 40 cathode-ray tubes of type C73376B and, for comparison, on 40 tubes of type 3KP1 chosen at random. Results indicated that the experimental tubes were somewhat inferior in this respect.

In September 1952, a tube removal program was initiated as one part of a preventive maintenance program. Since all of the troubles encountered had been the result of shorted or low emission tubes, it was believed that such a program would be helpful in eliminating a potential source of trouble. Blocks of tubes were removed at two-week intervals and were replaced by new ones. The location and number of tubes in a given block depended upon the area in which the most frequent troubles had been occurring. The number usually varied from 50 to 100. By 1954 ORDVAC had operated about 18,000 hours, and virtually all of its 3,000 tubes had been replaced at least once. The effect of the system of changing tubes by blocks was felt almost immediately and it was believed to be an important factor in the gradual increase of available time of machine operation.

While tube failures constituted the major cause of trouble in the ORDVAC, bad solder connections also were a cause of trouble. In one case a great many adder failures were eliminated by the discovery of a wiring error which had caused 200 volts to be applied between the heater and cathode of 50 tubes. Such errors were difficult to eliminate except through continued use of the machine.

Dust or dirt in the machine was also a problem. In almost any installation some dirt is certain to enter the cooling system regardless of any elaborate filtering that may be used. Simply exposing the components for necessary maintenance will allow a great deal of dust to enter a system. A computer using an electrostatic memory is especially susceptible to dust unless it is elaborately protected, because the high-voltage wiring forms a fine precipitator. This has been one of the great sources of trouble in the ORDVAC, not in the sense of actual occurrence of trouble, but in the sense of prevention of damage that might be done.

During the summer of 1952 sufficient dust had collected on the wiring so that the 2,000 volts arced to ground in a number of places. The damage included several clamping tubes that were exploded, at least six memory chassis that had to be replaced, and five cathode-ray tubes that were burned out. The arcing was eliminated by floating the high voltage system and supplying it with variable voltage, with high internal impedance. The arcs were both visible and audible in a darkened room and they were eliminated by cleaning and separating the wires where possible.

It is interesting to note that ORDVAC can be remotely controlled from commercial teletype units. This was actually used to solve problems for the University of Illinois. The University would send a program through regular teletype channels. It would then be placed in the ORDVAC after insuring that it had been received correctly. Answers were obtained on tape and returned to the University by mail or by the teletype channels. Thus the ORDVAC is available to any laboratory in the country having the necessary coding staff.

In July 1955 a 10,032-word magnetic drum was added to the ORDVAC memory system. The drum operates in a serial manner, that is, one bit at a time is transferred to or from the machine. The time required for the transfer of 48 words to or from the drum is from 50 to 70 milliseconds.

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When the magnetic drum was first installed track selection was made with relays, but these have since been replaced by a transistor track selector. Track selection time was reduced from 25 milliseconds to three microseconds.

On 8 June 1956 a 4,096-word magnetic core memory arrived for use on the ORDVAC. Almost four months were required to remove the old electrostatic memory and install the new magnetic core memory. Final acceptance tests were begun on 22 September 1956.

A new transistor adder was added to ORDVAC on 3 June 1958 and early in 1961 an index register was installed.

ORDVAC has operated on a 24 hour per day basis at better than 80% efficiency, and by late 1961 it was still scheduled to continue operation even after the newer machine, BRLESC would be in operation. (See Appendix III for technical data of ORDVAC.)

## **Chapter V -- BRLESC**

The capabilities of any given computer or computing system are never sufficient to solve all classes of problems efficiently and economically. There will always be a demand for faster arithmetic speed as well as for larger and faster memory. In fact, by 1955 the scientific computing facilities at the Ballistic Research Laboratory, APG, became unable to adequately support Ordnance requirements in the area of ballistic computations. The improved version of EDVAC and ORDVAC were laboring on a round-the-clock basis. The computer improvement programs which expanded the capability of these computers turned out to be only stop-gap measures. The existing machines were unable to adequately support the more than 100 active problems then being solved in the pursuit of ballistics research and the computation of firing tables and ballistic data for conventional artillery, rockets, and guided missiles. ENIAC was not able to keep up with EDVAC or ORDVAC and was no longer used after 2 October 1955. This placed the entire computation load on EDVAC and ORDVAC each of which operated 168 hours per week, with but a short time off each day for trouble shooting, repair, and improvements. Troubles over problem priority began to occur. Day-time computer runs were limited to twenty-minute program checks. Scramble time was a brief period of a few minutes for squeezing in a few high priority problems out of scheduled order. It was obvious that additional computer capacity was badly needed and this in the form of a computing machine that would be far superior to the existing machines.

The state of the art had advanced by 1957 to the point where superior machines were being developed by IBM, Sperry Rand, the Universities of Illinois and California, the Massachusetts Institute of Technology, and the National Bureau of Standards. Other companies and universities were also making rapid progress in the development and production of computing and data processing systems.

The decision was made to support the work of the National Bureau of Standards in exchange for the results of their development program and (in 1957) \$50,000 of Ordnance R&D funds were transferred to the National Bureau of Standards to assist in the development of universal logical packages which could be used in the construction of a new, fast, reliable, scientific computing machine. At that time the National Bureau of Standards was committed to the design of their new PILOT Multi-Computer

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System. The Ordnance funds assisted the Bureau of Standards in arriving at a tentative design of arithmetic, logical, and control units. The design and samples of the logical packages were provided to the Ballistic Research Laboratory at Aberdeen Proving Ground. Tests conducted at BRL showed that improvements in the design of the package were necessary. These modifications were approved by the Bureau of Standards and the sum of \$175,000 was transferred in February 1958, to the National Bureau of Standards to cover the cost of 6,000 of the packages to be ordered along with the Bureau's requirement for its PILOT Multi-Computer System. At the same time the programming staff of the Computing Laboratory at BRL prepared a description of the instructions to be automatically executed by the new computing machine. Due to the different types of application, the desire for easy programming and for reasons of economy, the Ballistic Research Laboratory at APG and the National Bureau of Standards parted ways in development. All that remained in common were the logical package and certain aspects of the high-speed arithmetic unit, which used the high-speed carry logic as proposed by the Bureau. The instruction code, physical construction, internal arrangement, control logic, peripheral equipment, and many other aspects differed. The logical design, physical design, and layout of the system was done independently by Computing Laboratory personnel at BRL.

The construction of plug-in units and racks was done under contract by the Technitrol Engineering Company of Philadelphia, PA. The development of the high-speed storage element was performed by Ampex Computer Products, Incorporated, of Culver City, CA (formerly Telemeter Magnetics, Inc.). The contract, approved by the Chief of Ordnance, called for the delivery of a 4,096-word storage unit with a cycle time of less than two microseconds. The operational unit, after some delays due to technical difficulties, was delivered to BRL on 15 May 1961 under Ordnance Contract No. DA-04-495-ORD-1500 at a total cost of \$680,000. Certain other components were also obtained under contract from various companies.

The assembly and logical wiring of the system was performed by Computing Laboratory personnel at BRL. This staff of computer engineers and programmers also conducted the checkout and testing of the system.

The new computing machine was named BRLESC, Ballistic Research Laboratory's Electronic Scientific Computer. It was designed by Ordnance personnel, for Ordnance Corps use, although in every respect it is a general purpose, high-speed, automatic computer. Its approximate ultimate cost is estimated at two million dollars. BRLESC was scheduled to be in operation by the end of 1961.

The BRLESC is an general purpose, electronic, digital computer with parallel arithmetic mode and synchronous timing. It was designed primarily for the solution of scientific problems in which high computational speed and high precision are required. As the descriptive phrase "general purpose" implies, the machine may be programmed to perform any task which is amenable to numerical methods of solution.

The applications of BRLESC are as follows:

1. Exterior ballistics problems such as high altitude, solar and lunar trajectories, computation for the preparation of firing tables and guidance control data for Ordnance weapons, including free flight and guided missiles.

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2. Interior ballistic problems, including projectile, propellant, and launcher behavior, e.g., physical characteristics of solid propellants, equilibrium composition, and thermodynamic properties of rocket propellants, computation of detonation waves for reflected shock waves, vibration of gun barrels and the flow of fluids in porous media.
3. Terminal ballistic problems, including nuclear, fragmentation, and penetration effects in such areas as explosion kinetics, shaped charge behavior, ignition, and heat transfer.
4. Ballistic measurement problems, including photogrammetric, ionospheric, and damping of satellite spin calculations, reduction of satellite doppler tracking data, and computation of satellite orbital elements.
5. Weapon systems evaluation problems, including antiaircraft and antimissile evaluation, war game problems, linear programming for solution of Army logistical problems, probabilities of mine detonations, and lethal area and kill probabilities of mine detonations, and lethal area and kill probability studies of missiles.

The binary number system is used exclusively in the arithmetic unit of the machine. The input-output routines (programs) automatically convert decimal input information into binary form and, conversely, convert binary numbers into decimal form for output. The arithmetic unit is constructed of standard vacuum tube logical packages, with tube driven, crystal diode logical gating. It contains 1,727 vacuum tubes of 4 types, 853 transistors of 3 types, 46,500 diodes of 2 types, and 1,600 pulse transformers of 1 type. Logical events are controlled by a five-phase megacycle clock, permitting decisions at the rate of five million per second.

The storage system of the machine consists of a high-speed magnetic core memory of 4,096 words. Each word is 72 bits long, which is equivalent computationally to approximately 19 decimal digits, since 4 parity bits and 4 sign bits are not included in the operands. The complete read-write cycle time of this memory is 1.5 microseconds. Additional high-speed storage will be added to the machine when funds become available. Also, magnetic drum storage units will be installed as back-up memory. The capacity of these drums is to be about 35,000 words.

The input-output devices of the machine are capable of reading cards, punching cards, reading magnetic tape, and recording on magnetic tape. A maximum of 16 magnetic tape handlers may be installed on line, that is, they are directly accessible to the programmer. Any two magnetic tape handlers, one drum, the card reader, and the card punch may be operated simultaneously under separate automatic controls. Arithmetic processing may occur concurrently with input-output operations. This means that information is processed automatically as it becomes available from an input device and automatic interlocks are built into the machine to insure that the proper information is available.

Information may be transferred to or from the machine by means of punched cards or magnetic tape. All information must be coded in a binary manner since the machine (as most modern computers) can only handle 0's and 1's, that is, hole or no hole, or magnetization in one direction or the other. The binary number system is used because of the binary nature of most of the devices used in the construction of the machine. The internal workings of the machine are simpler if only pure binary

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numbers and instructions are used. However, programmed routines can be designed to process any kind of information. The actual information may be a pure binary number, a binary coded decimal number, a binary coded alphabetic character, or literally any type of information the programmer desires. An output routine will arrange this information in the proper format for punched card output if desired, or for magnetic tape output. The punched cards may be tabulated on conventional punched card equipment and the magnetic tapes may be ready by special converter equipment which operates into a high-speed printer at rates up to 1,500 lines per minute, with 160 characters per line.

BRLESC was designed so that a maximum of concurrent operations can take place whenever possible. A "look-ahead of instructions, words, and indices" feature is incorporated to allow the machine to operate most effectively with a memory which cycles in one microsecond. Also, many special instructions may be executed while the arithmetic unit is working on an arithmetic instruction. In addition, all five input-output trunks may be operating simultaneously.

The control of BRLESC consists of many units, each controlling their associated process, but all regulated by a master control center, which has a pre-determined time priority system and which prohibits the initiation of new events in any of the various concurrent trunks should there be some conflict in the use of information or units. For example, if two tape trunks are to use the same tape handler for different purposes at the same time, the trunk which receives the first request gets priority to use the handler and the other trunk must wait until the first has finished using the handler. Also, should a program want to use information that has not arrived yet from one of five input-output trunks the master control center recognizes the problem and causes the program to wait until the information is delivered. The master control also recognizes manual commands from a console and then relays the commands to the respective sub-unit.

Magnetic tape speeds operate at an effective rate of 120,000 six-bit characters per second. Search through magnetic tape in the forward or backward direction by large blocks of information is an incorporated feature. New programs can be located rapidly through the use of file markers. Drum transfer rates are 130,000 seventy-two-bit words per second.

BRLESC is provided with a parity system to check word transfers as they pass through the memory and to or from tapes and drums. The master control unit is altered in the event a non-parity condition occurs.

The computer is designed to operate on an internally stored program of detailed instructions. This feature is the single, most important reason for the tremendous growth of the computer industry, because it makes computers truly flexible and easy to use. Since instructions are in numerical form, arithmetic operations may be performed on them, that is they may be manipulated in the arithmetic unit. In this way the program can modify its own instructions during the course of the computation in response to conditions that develop. This allows the programmer to exercise his ingenuity and gives him latitude to do many things without writing a great many detailed instructions.

Another very valuable feature is that the machine can change address in instructions by fixed amounts automatically. This feature is called indexing and permits the programmer to use the same set of instructions to process as much data as he desires simply by changing the index value instead of modifying the basic instructions.

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Code checking features will include stopping on any selected address, the display of the contents of any memory cell, the display of normal or abnormal conditions, the ability to manually store in any selected memory cell, and the ability to transfer control to any part of the system. Parity checking is performed in each of the four 17-bit groups in each word.

It is believed that BRLESC will be a significant contribution to the Ordnance Corps and to the scientific community, because it will permit the solution of problems never before possible due to the excessive amount of time required; and it will solve these problems at a precision which was possible on earlier machines only by complicated, time-consuming methods. (See Appendix IV for technical data of BRLESC.)

## **CHAPTER VI -- COMPUTERS FOR SOLVING GUNNERY PROBLEMS**

The ever present need of the field artillery is a means to solve the gunnery problem with greater accuracy and speed. Tactical requirements are changing constantly at a mounting tempo, with increasing demands being placed upon field artillery in its support of the field army. This is a continuous challenge in the area of fire control where new techniques are being devised, the newest advances in science are being adapted and applied, qualified personnel are being trained for new jobs, and where field artillery is finding the means for meeting the demands for its increased support.

The development and standardization of the Field Artillery Fire Control System M35 was a significant step in the right direction. This system utilized an electromechanical computer and opened a new era in gunnery techniques. The Fire Control System M35 was an improvement over graphical means in both speed and accuracy, but experience with it also pointed to needs for improvement in the over-all fire control problem. The analog system used by this device had several disadvantages. Its accuracy was adequate for the shorter range weapons such as the 105-mm and 155-mm howitzers, but was not adequate for guns and free rockets. It was clear that a system of computing was needed which would be more flexible than was possible with an analog system. Ordnance and CONARC agencies cooperated to establish the actual requirements and definitions of problems, and from these Ordnance was able to specify and develop the needed equipment.

Frankford Arsenal studied the basic ballistic problem for about two years and then the Univac Division of Remington Rand studied the problem along with its associated mathematics. The most desirable approach appeared to be simulation of the flight of the projectile from the tube (launcher) to impact, which is referred to as solving the differential equations of motion of the projectile. After reaching an acceptable mathematical solution, the next major problem was the incorporation of this solution into a device compatible with the size, weight, power maintenance requirements, and operation training imposed by the field artillery.

In November 1956 a conference was held at Frankford Arsenal to present the solution and concept of mechanization. This concept was called the Field Artillery Digital Automatic Computer (FADAC). Military Characteristics were drafted and approved. The design criteria for a machine were submitted to industry and a contract placed with Autonetics, a division of North American Aviation, Inc., on 20

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June 1958 for the design, development, and manufacture of FADAC. Target schedules called for acceptance tests by Frankford Arsenal in September 1959 of the first prototype FADAC.

The basic considerations and order of priority in arriving at the design of the hardware for FADAC were established as:

1. Accuracy of solution and reliability of operation.
2. Ruggedness (ability to withstand adverse climate and field conditions).
3. Minimal operation (computing time).
4. Ease of operation and operator training.
5. Ease of maintenance and maintenance personnel training.
6. Minimum physical size, weight, and power consumption (not to exceed 200 lb in weight and 500 w in power.)
7. Cost.

The FADAC is a solid-state electronic digital computer. It is compact, portable, and rugged. It is approximately 24 x 14 x 34 inches in size and weighs about 200 pounds. It is designed to operate under severe field conditions and storage, and under extreme temperatures of heat and cold. For use by the fire direction center, FADAC requires only the addition of 3-phase 400-cycle power to the fire direction center facilities.

Transistors are used throughout FADAC circuits. Crystal diodes are used for logical gating. The machine is a stored-program, solid-state (no vacuum tubes), electronic digital computer to be used primarily for automatic computing and visual displaying of firing data (gun orders) for Field Artillery weapons, from inputs defining target and weapon locations together with nonstandard conditions of materiel and weather.

It will provide firing data for a battery of weapons. On a one-battery- at-a-time basis, it can provide firing data for mortars, howitzers, guns, and free rockets, firing any ammunition these weapons will use. In emergencies, it can provide data for five similar type batteries, one at a time. By using the memory loading unit, authorized field personnel can make program changes to permit solution of gunnery problems for other weapons in a few minutes time.

Parts, sub-assemblies, and support equipment are interchangeable with any other FADAC, regardless of weapon or the application to which each may be assigned.

The flexibility of FADAC is demonstrated in the interchangeable control sections, each designed for a particular use. The use of FADAC with different weapons and for different applications is facilitated by changing control sections. For example, a gunnery problem could be solved by FADAC using the control section designed for gunnery, and then the control section could be changed for a counter-

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battery problem. A removable plug in the control section simplifies such changes. This design is not only a flexible operating feature, but also one that minimizes operator training.

FADAC was designed for high operational dependability and for maintenance to be required only at infrequent intervals. It should be capable of operating under field conditions, without major overhaul, for at least 2,500 hours. The solid-state components are expected to operate for at least 10,000 hours. Errors due to internal malfunctions during a computation will be minimized by internal automatic monitors which aid in detecting such errors.

FADAC was designed to be compatible for transmission purposes with the fielddata family of equipment under development by the Signal Corps as part of the Automatic Data Processing System (ADPS) program. The basic difference between the fielddata code and the teletype system is that the former requires more pulses to transmit a greater amount of information, i.e., an 8-level instead of a 5-level system. Of the 8 levels, 6 are used for information or intelligence, 1 for parity or to check the transmission of the data, and 1 bit for a control-type function. The FADAC can transmit and receive this 8-level fielddata code.

Input consists of a manual keyboard and various arrangements of paper tape or another FADAC. When all the data, such as target location, powder temperature, gun location, and meteorological data, are entered, depression of a button initiates computation. Gun orders, comprising deflection, quadrant elevation, fuze time, and charge are displayed in decimal form.

Output consists of visual display (called Nixie), another FADAC, battery display, printer, magnetic tape, fielddata equipment, and teletype equipment.

The programming and numerical system of FADAC is straight binary for internal operations, with automatic conversions to other codes for input- output.

In the arithmetic unit the execution time for each instruction is 7.8 microseconds. Its arithmetic mode is parallel by function and serial by bit. Timing is synchronous.

The storage consists of a main magnetic disc of 4,096 word capacity and a high-speed magnetic disc of 32 word capacity. There are 32 channels of 128 words each, of which 24 channels are designated as permanent storage and 8 channels as working storage.

The extremely high-speed operation of this machine is made possible by a combination of new techniques incorporated in the logic design. While FADAC is basically a serial computer, it performs some functions in parallel, that is, several operations simultaneously. Instruction search, instruction interpretation, number search, and number read are performed at the same time. This overlapping feature, together with minimum access coding, rapid access loops, and multiplication using two bits at a time, results in a machine capable of performing 12,800 additions or subtractions per second, approximately 750 multiplications per second, and 375 divisions per second, including access time for both instructions and numbers.

There are several additional applications of FADAC. One of these is as an ideal replacement for JUKEBOX as a computer for the Redstone Missile System. Frankford Arsenal had developed

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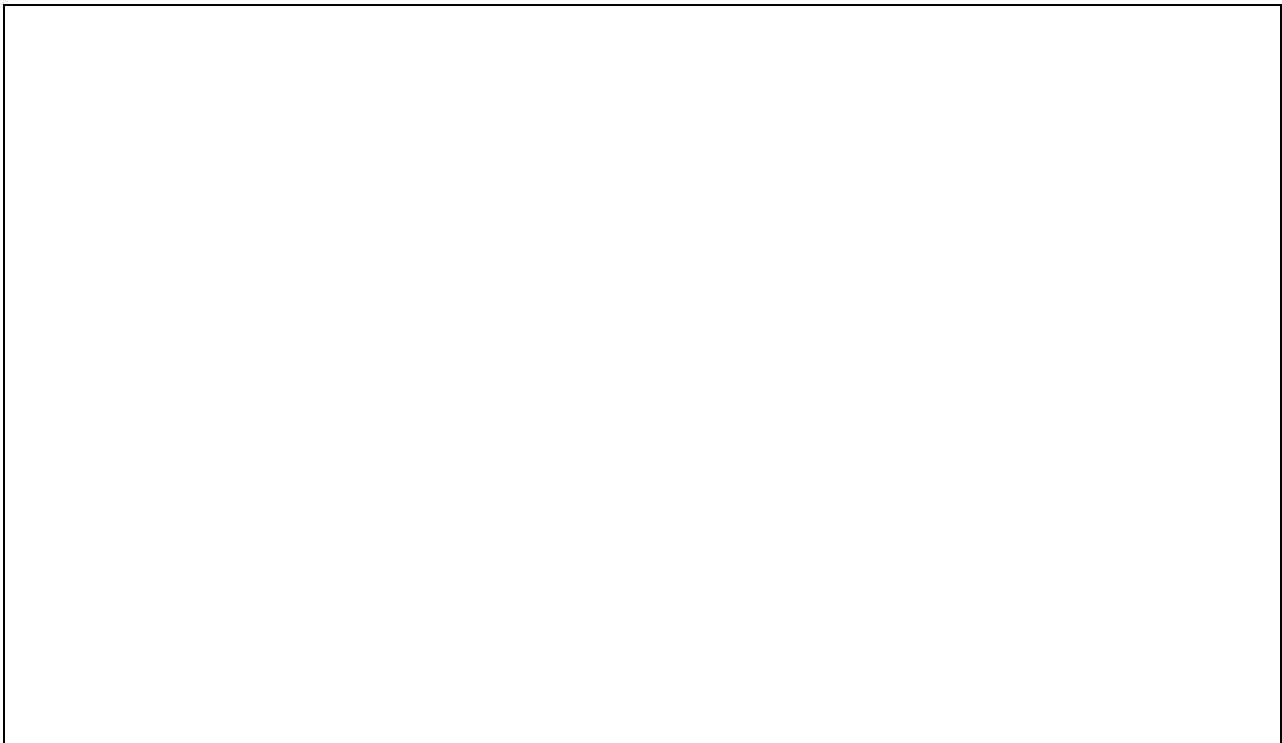
JUKEBOX before the development of FADAC had started, but, while an excellent computer, it was designed for vehicle mounting and operation where size, weight, and power were not of prime importance. FADAC can meet all of the requirements and have the advantage of smaller size and weight.

Other missile systems could also use FADAC. These are: Pershing, Sergeant, Lacrosse, and NIKE-Hercules. In addition to the missile systems FADAC can also be employed in fire planning, survey computations, counter- battery computation, reduction of metro data, and as universal automatic check-out equipment.

A universal computer for solving all gunnery problems has always seemed to lie in the future. However, continuous study at Frankford Arsenal on increasing the utility and application of FADAC has yielded results which make this computer a candidate for the title "Universal Field Artillery Computer".

(The material for this chapter was extracted from Frankford Arsenal Technical Memorandum Report M59-5-1, "FADAC Status Report," by R. Brochman, dated 29 December 1958.)

## **CHAPTER VII -- THE COMPUTER TREE**



1280x1024 version of this image (99 Kbytes).

FULL-SIZE 400dpi version of this image (1.2 Mbytes).

The computer tree shows the evolution of electronic digital computers. The automatic computing and data processing industry is a direct outgrowth of research, sponsored by the U.S. Army Ordnance

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Corps, which produced the ENIAC, the world's first electronic digital computer. This industry has grown to a multi-billion dollar activity that has penetrated every profession and trade in government, business, industry, and education.

In the accompanying graphical representation of the computer tree the trunk rests on the ENIAC. The serial computers, represented by EDVAC, and the parallel computers, represented by the ORDVAC, are shown as separate limbs. This separation tends to distinguish the business computers on the left limb from the scientific computers on the right limb. The computers which were developed specifically to meet military needs are shown on the center limb. Manufacturers have entered the electronic computer field at different times, shown as various branches. Only university and government sponsored computers are shown along the limbs. The radial distance from the ENIAC is an approximate indication of the year each computer was developed, constructed, or placed in operation.

The impact of computers is tremendous. Our lives are certainly influenced by these automatons, and our very production of consumer and defense goods is indirectly controlled by them. Our national defense is entrusted to them. Our inventories and stock keeping are controlled, our records are kept, our bookkeeping is performed by them. Our routine, tedious, and painfully repetitive mental effort is ameliorated by them. We are relieved of arduous mental tasks by them much the same as we were relieved of arduous manual tasks by powered machinery. We are on the threshold of a new era and computing machines are here to stay and play an ever greater part in this era.

The computing machines described in this monograph are merely the beginners. They are the counterparts of the devices of the Howes, the Wrights, the Marconis, the Bells, and the Edisons, although they appear super-modern to us at this time. Nevertheless they are the machines which opened a new frontier in human endeavor with seemingly unlimited capabilities and applications.

(For example, research is being conducted at Frankford Arsenal on automatic checkout systems for combat vehicles, missile checkout systems, and automatic diagnostic equipment of a very sophisticated type.)

## **APPENDIX I -- ENIAC**

### ENIAC

Electronic Numerical  
Integrator and Computer

MANUFACTURER  
Moore School of  
Electrical Engineering  
University of Pennsylvania

OPERATING AGENCY  
U.S. Army Ordnance Corps  
Ballistic Research Laboratories  
Aberdeen Proving Ground, MD

# ELECTRONIC COMPUTERS WITHIN THE ORDNANCE CORPS HISTORICAL MONOGRAPH FROM 1961

Karl Kempf  
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## GENERAL SYSTEM

Applications Solution of ballistic equations, fire control problems, data reductions, and related scientific problems.

Timing                    Synchronous  
Operation                Sequential

## NUMERICAL SYSTEM

Internal Decimal in basic computer, binary coded decimal in magnetic storage.

Decimal digits per word 10 plus sign  
Decimal digits per instruction 2  
Instructions per word 5 or 6  
Total no. of instructions decoded 100  
Total no. of instructions used 97  
Arithmetic system            Fixed-point  
Instruction type              One-Address Code  
Number range                 $10^{-10}$  -1 to  $1-10^{-10}$

## ARITHMETIC UNIT

Add time (excluding storage access) 200 microsec  
Multiply time ( " " " ) 2,800 microsec  
Divide time ( " " " ) 24,000 microsec  
Construction: Vacuum-tubes  
Number of rapid access word registers 120  
Basic pulse repetition rate 60-125 kilocycles/sec variable.  
Arithmetic Mode: Parallel

Information is transferred in parallel as a serial train of pulses.

## STORAGE

Media	Words	Microsec Access
Vacuum-tubes	20	200
Magnetic core	100	200
Function table	304	lines of 12 dec digits + sign on each constant set-switch
Plug board	96	lines of 12 dec digits + sign each (IBM)
Relays	8	buffer capable of storing contents of one card

## INPUT

Media                            Speed  
IBM Cards                    125 cards/min

Each card has 8 ten decimal digit words plus signs.

## OUTPUT

Media                            Speed

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IBM Cards 100 cards/min

200 millisecc of card cycle are available for other computer operations. At 50 cards/min rate, 800 millisecc are available for computer operations per card cycle.

## NUMBER OF CIRCUIT ELEMENTS

Tubes	17,468
Tube types	16
Crystal diodes	7,200
Magnetic elements	4,100

## PHYSICAL FACTORS

Power consumption, Computer	174 K.W.
Space occupied, Computer	1,800 sq ft
Air conditioning	Forced outside air.

## MANUFACTURING RECORD

Number produced	1
Number in current operation	1

## COST

Additional equipment	Magnetic storage
\$29,706.50	
Rental rates for additional equipment:	
I.B.M. card reader	\$82.50 per month
I.B.M. card punch	\$77.50 per month
Approximate cost of basic system	\$750,000

## PERSONNEL REQUIREMENTS

Daily operation	No. of Tech.
3 - 8 hour shifts	6
7 days/week	

A minimum requirement of operation and servicing on a 24-hour-day, 7-day- week basis. No engineers are assigned to operation of the machine, but they are used for design, development of improvements and consultation when total breakdowns occur.

## RELIABILITY AND OPERATING EXPERIENCE

Date unit passed acceptance test	1946
Average error free running period	5.6 hrs
Operating ratio 0.69	Good time 113 hrs
(Figures for 1955) Attempted to run	164 hrs/wk
No. of different kinds of plug-in units	44
No. of separate cabinets (excluding power and air cond.)	42
Operating ratio figures for 1954:	
Operating ratio 0.70	Good time 116 hrs
Attempted to run	166 hrs/wk

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## ADDITIONAL FEATURES AND REMARKS

There are four modes of operation: Continuous, Pulse time, Add time, or Instruction time.

A manual pre-set stop box is available.

Count instructions and transfer instructions are used.

## APPENDIX II -- EDVAC

EDVAC

Electronic Discrete Variable Automatic Computer (U.S. Army Photo)

### APPLICATIONS (Ballistic Research Laboratories)

Exterior ballistics problems such as high altitude, solar and lunar trajectories, computation for the preparation of firing tables and guidance control data for Ordnance weapons, including free flight and guided missiles.

Interior ballistic problems, including projectile, propellant and launcher behavior, e.g., physical characteristics of solid propellants, equilibrium composition and thermodynamic properties of rocket propellants, computation of detonation waves for reflected shock waves, vibration of gun barrels and the flow of fluids in porous media.

Terminal ballistic problems, including nuclear, fragmentation and penetration effects in such areas as explosion kinetics, shaped charge behavior, ignition, and heat transfer.

Ballistic measurement problems, including photogrammetric, ionospheric, and damping of satellite spin calculations, reduction of satellite doppler tracking data, and computation of satellite orbital elements.

Weapon systems evaluation problems, including anti-aircraft and anti-missile evaluation, was game problems, linear programming for solution of Army logistical problems, probabilities of mine detonations, and lethal area and kill probabilities of mine detonations, and lethal area and kill probability studies of missiles.

### PROGRAMMING AND NUMERICAL SYSTEM

Internal number system	Binary
Binary digits per word	44
Binary digits per instruction	4 bits/command
10 bits each address	
Instruction per word	1
Instructions decoded	16
Instruction used	12
Arithmetic system	Floating and Fixed point
Instruction type	Four-address code

EDVAC Floating Point (U.S. Army Photo)

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HISTORICAL MONOGRAPH FROM 1961**

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## Number range

### Fixed

-(1-2<sup>43</sup>) less than or equal to n less than or equal to (1-2<sup>43</sup>)

### Floating

-(1-2<sup>33</sup>)2<sup>511</sup> less than or equal to n less than or equal to (1-2<sup>33</sup>)2<sup>511</sup>

The fractional part of floating point number has 33 bits plus sign, and the exponent of 2 may range from -512 to +511.

## Instruction word format

Alpha-Add	Beta-Add	Gamma-Add	Delta-Add	Order
1-10	11-20	21-30	31-40	41-44

## ARITHMETIC UNIT

Add time (includ. stor. access) (min 192 max 1,536)	Microsec	864
Mult time (includ. stor. access) (min 2,208 max 3,552)		2,880
Div time (includ. stor. access) (min 2,256 max 3,600)		2,930
Construction	Vacuum-tubes and Diode-gates	
Number of rapid access word registers		4
Basic pulse repetition rate		1.0 megacycle/sec
Arithmetic mode	Serial	
Timing	Synchronous	
Operation	Sequential	

## STORAGE

Media	Number of Words	Number of Digits	Access Microsec
Mercury A.D.L.	1,024	48-384	48-384
Magnetic Drum	4,608	48/Word	17,000

Includes relay hunting and closure.

The rate of information transfer to and from the drum is at one megacycle per second. The block length is optional from 1 to 384 words per transfer instruction.

Magnetic tape	48/Word	
Maximum number of units that can be connected to the system		7 Units
Maximum number of characters per linear inch of tape		112 Char/inch
Channels or tracks on the tape		8 Track/tape
Blank tape separating each record		1.5 Inches
Tape speed		75 Inches/sec

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Start time	3 Milliseconds
Stop time	3 Milliseconds
Average time for experienced operator to change reel of tape	30 Seconds
Physical properties of tape	
Width	5/8 Inches
Length of reel	1,250/2,500 Feet
Composition	Red Oxide

The magnetic tape system has the following features: Variable block length from 2 to 1,024 words. The search order releases the machine for computation during search. Information which has been taken from a block and operated upon, can be automatically re-recorded in the same block.

## INPUT

Media	Speed
Photoelectric Tape Reader	942 sexadec char/sec 78 words/sec
Card Reader (IBM)	146 cards/min 8 words/card

## OUTPUT

Media	Speed
Paper Tape Perf.	6 sexadec char/sec 30 words/min
Teletypewriter	6 sexadec char/sec 30 words/min
Card Punch	125 cards/min 1,000 words/min

## CIRCUIT ELEMENTS OF ENTIRE SYSTEM

Type	Quantity	Type	Quantity
Tubes, total	5,937		
6Y6	1,000	6AN5	275
6J6	1,500	2D21	160
6AG7	1,127	6SN7	150
6V6	900	6AS6	50
6L6	275	Misc	500
Diodes, total	12,000		
1N297	6,000	Misc	1,200
1N 34	4,800		
Transistors, total	328		
2N398	256	2N123	4
2N1008B	60	2N167	4
2N 43	4		

## CHECKING FEATURES

Two arithmetic units perform computation simultaneously, discrepancies halt machine. Unused commands halt machine. Paper tape reader error detection.

# ELECTRONIC COMPUTERS WITHIN THE ORDNANCE CORPS HISTORICAL MONOGRAPH FROM 1961

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## POWER, SPACE, WEIGHT, AND SITE PREPARATION

Power, computer	52 K.W.
Space, computer	490 sq. ft. floor
Weight, computer	17,300 lbs.
Power, air cond.	25 K.W.
Space, air cond.	6 sq. ft. floor
Weight, air cond.	4,345 lbs.
Capacity, air cond	20 Tons

## PRODUCTION RECORD

Number produced	1
Number in current operation	1

## COST, PRICE, AND RENTAL RATES

Approximate cost, basic system	\$467,000
Rental rates for additional equipment	
I.B.M. card reader	\$82.50 per month
I.B.M. card punch	\$93.50 per month

## PERSONNEL REQUIREMENTS

Typical Personnel	Three 8-Hour Shifts
Supervisors	6
Analysts	3
Programmers and Coders	14
Clerks	1
Engineers	1
Technicians	6

No engineers are assigned to the operation of the machine, but are used for development and design of additions to the machine. The technicians consult the engineers when a total break-down occurs.

## RELIABILITY, OPERATING EXPERIENCE, AND TIME AVAILABILITY

Average error-free running time	Approx. 8 hours
Good time	145 hours/week
Attempted to run time	168 hours/week
Operating ratio	0.87

Figures based on last 3 years. The 23 hours per week are devoted to scheduled and unscheduled maintenance, testing, modifications and improvements, time lost due to error, etc. The 145 hours are good, useful production time. EDVAC has been operating since 1949.

## ADDITIONAL FEATURES AND REMARKS

- Oscilloscope and neon indicator for viewing contents of any storage locations at any time.
- Exceed capacity options: halt, ignore, transfer control, or go to selected location.
- Unused instruction (command) halt.

# **ELECTRONIC COMPUTERS WITHIN THE ORDNANCE CORPS HISTORICAL MONOGRAPH FROM 1961**

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- Storage of previously executed instruction and which storage location it came from, for viewing during code checking.
- Storage of current instruction and storage location it originated from.
- Address halt when prescribed address appears in any of 4 addresses of instruction to be executed by computer.
- Tape reader error detection.
- Built in automatic floating point equipment.
- Magnetic tape auxiliary storage unit and high speed printing techniques are being investigated.
- Punching one card requires from 384 to 768 microseconds. The computer may proceed between cards.

## **INSTALLATIONS**

Ballistic Research Laboratories  
Aberdeen Proving Ground, MD

## **FUTURE PLANS**

A second magnetic drum system, of 16,128 words capacity is being added to the EDVAC. The transistorized track selector will permit channel switching in 48 microseconds. Synchronous Magnetic Drum (U.S. Army Photo)

## **APPENDIX III -- ORDVAC**

ORDVAC Ordnance Variable Automatic Computer (U.S. Army Photo)

### **APPLICATIONS (Ballistic Research Laboratories)**

Exterior ballistics problems such as high altitudes, solar and lunar trajectories, computation for the preparation of firing tables and guidance control data for Ordnance weapons, including free flight and guided missiles.

Interior ballistic problems, including projectile, propellant, and launcher behavior, e.g., physical characteristics of solid propellants, equilibrium composition and thermodynamic properties of rocket propellants, computation of detonation waves for reflected shock waves, vibration of gun barrels and the flow of fluids in porous media.

Terminal ballistic problems, including nuclear, fragmentation and penetration effects in such areas as explosion kinetics, shaped charge behavior, ignition, and heat transfer.

Ballistic measurement problems, including photogrammetric, ionospheric, and damping of satellite spin calculations, reduction of satellite doppler tracking data, and computation of satellite orbital elements.

# ELECTRONIC COMPUTERS WITHIN THE ORDNANCE CORPS HISTORICAL MONOGRAPH FROM 1961

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Aberdeen Proving Ground, MD

Weapon systems evaluation problems, including anti-aircraft and anti-missile evaluation, war game problems, linear programming for solution of Army logistical problems, probabilities of mine detonations, and lethal area and kill probabilities of mine detonations, and lethal area and kill probability studies of missiles.

Transistorized Arithmetic Unit (U.S. Army Photo)

## PROGRAMMING AND NUMERICAL SYSTEM

Internal number system	Binary
Binary digits per word	40
Instructions per word	2
Instruction type	One Address
Binary digits in operation code	6 or 9
Binary digits in address	12 or 10
Instructions used	55 or 72
Arithmetic system	Fixed point
Number range	-1 less than x less than 1

Instruction word format					
Left Instruction			Right Instruction		
6	2	12	6	2	12
Order	Unused*	Address	Order	Unused*	Address
20 Bits			20 Bits		

\*One bit will be used to differentiate floating point numbers from fix point numbers

Rapid Access word registers - 3  
Sexadecimal representation is used externally.  
Negative numbers are handled as 2 complements.  
Floating point operation may be programmed.

Dual code - ORDVAC operates on a dual code basis. The codes are, on a two instructions per word basis, i.e., 20 digits per instruction:

Code A - 1,024 words of storage:  
9 digit, command  
1 digit, spare  
10 digit, address  
Code B - 4,096 words of storage:  
6 digit, command  
2 digit, spare  
12 digit, address

This system permits utilization of routines developed previous to the 4,096-word operation change over.

Magnetic core memory (U.S. Army Photo)

## ARITHMETIC UNIT

Arithmetic mode	Parallel
Basic pulse rate	Not pulse controlled

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Add time (basic addition by arithmetic unit)	14 microsec
Multiply time (exclud. stor. access)	700 microsec
Divide time (exclud. stor. access)	700 microsec

The total add time, including transfer to final register, is 50 microseconds. None of the above figures include access to storage.

Construction, Arithmetic unit only - Transistorized on printed circuit plug-in boards, using 1,000 Type 2N128 transistors.

Timing Asynchronous  
Operation Parallel

Transistorized Channel Selector (U.S. Army Photo)

## STORAGE

Media	Words	Digits	Access
Magnetic core	4,096	163,840 bits	15 microsec
Magnetic drum	10,032	401,280 bits	80,000 microsec /48 words

Magnetic drum purchased from ERA Division of Sperry Rand, Incorporated. The Track selector for the magnetic drum has been transistorized. Magnetic core storage unit purchased from Telemeter Magnetics, Incorporated. Both above storage units adapted to ORDVAC and installed by Ballistic Research Laboratories personnel.

## INPUT

Media	Speed
Teletype tape (5 hole)	2.5 words per sec
Punched cards	40 words per sec (bin) 8 words per sec (dec)
Ferranti Hi-speed Paper Tape Reader	20 words per sec (bin)
Magnetic tape	300 words per sec

The special purpose one inch wide magnetic tape system for transferring telemetered data to ORDVAC has 6 information tracks and 3 control tracks.

## OUTPUT

Media	Speed
Teletype page printer	0.4 words per sec
Teletype tape	0.4 words per sec
Punched cards	40 words per sec (bin) 8 words per sec (dec)

Transistorized magnetic core contents display.

## CIRCUIT ELEMENTS OF ENTIRE SYSTEM

Tubes			
Type	Quan	Type	Quan
5964	817	C6J	28
5687	420	6X5	4

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2C51	568	0C3	4
5965	637	6SF5	4
6AL5	47	6AC7	4
6A67	2	12SN7	12
2D21	160	12AU7	1
6080	21	6AH6	9
6AN5	13	6350	86
0B2	14	6829	2
7AK7	16	6216	2
5963	46	6BJ7	42
6AV6	13	6197	90
5R4	2	6293	193
6L6	26	5998	72
12AX7	22	6336	27
6X4	6	350B	4
5651	12	0A2	3
			-----
6AQ5	1	Total	3,430

## Transistors

Type	Quan	Type	Quan
2N162	20	2N1056	250
2N140	65	2N113	75
2N128	1,300	2N426	25
2N109	346	2N425	10
			-----
		Total	2,091

## Diodes

Type	Quan	Type	Quan
1N91	418	1N63	15
1N93	162	1N58A	10
1N52	10	1N298	300
			-----
		Total	915

## POWER, SPACE, WEIGHT, AND SITE PREPARATION

### Power Consumption

Computer	40 K.W.
Core Memory	15 K.W.
Magnetic Drum	6 K.W.

### Air Conditioning

Computer	15 Tons
Core Memory	7.5 Tons
Magnetic Drum	3 Tons

### Space

Computer	630 cu ft	80 sp ft
----------	-----------	----------

### Weight

Computer	3,000 lbs
----------	-----------

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## PRODUCTION RECORD

Number produced to date	1
Number in current operation	1

## COST, PRICE, AND RENTAL RATES

Rental rates for additional equipment \$648.57 per month  
The additional rented equipment is:  
I.B.M. punch \$ 83.32 per month  
I.B.M. reader \$ 82.50  
I.B.M. reproducer \$122.50  
I.B.M. tabulator \$360.25  
Approximate cost of basic system \$600,000.

## PERSONNEL REQUIREMENTS

Typical Personnel	Three 8-Hour Shifts
Supervisors	6
Analysts	3
Programmers and Coders	14
Clerks	1
Engineers	1
Technicians	6

No engineers are assigned to the operation of the machine, but are used for development and design of additions to the machine. The technicians consult the engineers when a total break-down occurs.

## RELIABILITY, OPERATING EXPERIENCE, AND TIME AVAILABILITY

Average error-free running period	Approx. 6 hours
Good-time	7,475 hours
Attempted to run time	8,760 hours/year
Operating ratio	0.85

The above figures are based on the yearly average of the last 5 years. Approximately 2 hours per week are used for scheduled preventive maintenance and 10 hours per week are used for running computer test programs. The 1,286 hours difference above were used for testing, servicing, bad operating time, general improvement, and the incorporation of new components.

## ADDITIONAL FEATURES AND REMARKS

The ORDVAC belongs to the group of computers whose basic logic was developed by the Institute for Advanced Study and utilized in the IAS computer. This IAS family of computers is made up of such machines as the ILLIAC, ORACLE, AVIDAC, MANIAC, JOHNNIAC, MISTIC, and CYCLONE.

The ORDVAC is a direct-coupled machine using three-dimensional construction. A direct-coupled machine is one that connects the voltage level of one component directly to the input of the next, without voltage isolation between. This feature is very helpful in trouble-shooting the system. Three-dimensional construction is sometimes called low-capacitance wiring. In the ORDVAC, three-dimensional wiring is employed by placing the arithmetic unit and other controls on opposite sides,

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and interconnected wiring running across the open space between. The machine can be remotely controlled from commercial Teletype units.

ORDVAC is equipped with the option of two different instruction codes. Code -9 (nine bits per instruction) makes 1,024 words of high speed core storage available to the operator while Code -6 (six bits per instruction) makes 4,096 words of high speed storage available. Each code shares a common nine-bit decoder; however, when the code -6 option is used the instruction first passes through a code translator which translates the six bit instruction into its 9-bit equivalent. There is no loss of time while making the code translation.

The translator uses the following number of circuit elements.

Transistors	
SB 100	135
2N 43	24
2N 140	12
	----
Total	171
Crystal diodes	253
Resistors	305
Capacitors	23

The above components are mounted on 21 printed circuit boards. Power dissipation is approximately 5 watts.

## INSTALLATIONS

Ballistic Research Laboratories  
Aberdeen Proving Ground, MD

## FUTURE PLANS

The Floating Point unit for the ORDVAC will be fully transistorized, with a number range of  $2^{127}$  to  $2^{-128}$ , using a seven bit biased exponent. Numbers will be normalized automatically on transfer to storage. The mantissa of the normalized floating-point number will have a range of  $1/2$  greater than  $c$  greater than  $-1/2$ . This system will require that an existing register be converted from a one-sided shifting register to a two-sided shifting register.

Fully transistorized control circuitry for new indexing orders will be added in the near future.

General purpose magnetic tape stations will be added to the ORDVAC shortly, with provisions for 8 stations. ORDVAC will control read, write, re- wind forward and backward, move tape forward and back N words, starting at A address of memory, transfer to B address of memory for next instruction, re- record N words, playback N words, check for parity error, transfer on error, and other functions.

## Circuit Elements, Entire System

Magnetic Cores			
Quan	OD	ID	Thick
172,032	100	70	30 mils

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5,376      375      260      125      mils

## APPENDIX IV -- BRLESC

BRLESC Ballistic Research Laboratories Electronic Scientific Computer  
(U.S. Army Photo)

### APPLICATIONS

Exterior ballistics problems such as high altitude, solar and lunar trajectories, computation for the preparation of firing tables and guidance control data for Ordnance weapons, including free flight and guided missiles.

Interior ballistic problems, including projectile, propellant and launcher behavior, e.g., physical characteristics of solid propellants, equilibrium composition and thermodynamic properties of rocket propellants, computation of detonation waves for reflected shock waves vibration of gun barrels and the flow of fluids in porous media.

Terminal ballistic problems, including nuclear, fragmentation and penetration effects in such areas as explosion kinetics, shaped charge behavior, ignition, and heat transfer.

Ballistic measurement problems, including photogrammetric, ionospheric, and damping of satellite spin calculations, reduction of satellite doppler tracking data, and computation of satellite orbital elements.

Weapon systems evaluation problems, including antiaircraft and anti-missile evaluation, war game problems, linear programming for solution of Army logistical problems, probabilities of mine detonations and lethal area and kill probabilities of mine detonations, and lethal area and kill probability studies of missiles.

### PROGRAMMING AND NUMERICAL SYSTEM

Internal number system	Binary							
Binary digits/word	68 + 4 parity							
Binary digits/instruction	68							
Instructions/word	1							
Instructions decoded	33							
Arithmetic system	Fixed and floating point							
Instruction type	Three-address							
Instruction word format								
4	4	6	14	6	14	6	14	
Order type	Para-meter	Index	(alpha)-Ad-dress	Index	(beta)-Ad-dress	Index	(gamma)-Ad-dress	
Number word format	Fixed Point							
3	1	4	.	60				
Tag	Sign	Binary Point						
Number word format	Floating Point							
3	1	4	.	52	8			
Tag	Sign	Binary Point		Coefficient	Biased Exp of 16			

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## Automatic built-in subroutines

In addition to the standard set of jump instructions, three more jump instructions have been included which will be used in connection with the "permanent" storage of "built-in" subroutines. These are Jump to "permanent" instruction, Jump to "built-in" subroutine, and Set index and jump to main memory.

## Registers and B-boxes

The machine will have 63-one microsecond access index registers, addressable by the alpha, beta, and gamma addresses of the instruction words.

The parameter bits of the instruction word are used to indicate variations of the basic order type.

All three arithmetic registers are 68 bits. Tag bits enter these registers only on the logical instructions and the shift instruction if it is cyclic or is a Boolean shift. On arithmetic orders, the tag bits are saved in a separate three bit register and the three extra bits in the arithmetic registers are used for checking overflow. Thus the range of numbers in the arithmetic unit is -128 less than or equal to N less than 128.

Add and subtract are performed the same as for normalized arithmetic, except the result is never shifted left at the end of the operation.

Before multiply is done, the coefficient that has the largest absolute value is normalized. There is no left normalization after the operation. Thus the result has approximately the same number of significant digits as the operand that had the smaller number of significant digits. It does tend to retain an average of about two or more bits than it should, however.

Before divide is done, both operands are normalized but the number of divide steps performed is reduced accordingly so that the result has approximately the same number of significant digits as the operand that had the smaller number of significant digits.

## ARITHMETIC UNIT

Operation	Microseconds			
	Excl	A	T	Incl A T
Fixed point add or subtract		1		5
Fixed or floating multiply		20		25
Fixed or floating divide		60		65
Floating add or subtract	3.0			6
Boolean logic operation		1		5
Indexing and control		2		2 (Avg)

## Construction (Arithmetic unit only)

The arithmetic unit is constructed of standard vacuum tube logical packages, with tube driven, crystal diode logical gating. The arithmetic unit only is constructed of 1,727 vacuum tubes of 4 types, 853 transistors of 3 types, 46,500 diodes of 2 types and 1,600 pulse transformers of 1 type.

Arithmetic mode                      Parallel

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Timing Synchronous

Logical events are controlled by a five-phase clock, permitting decisions at a 5 Mc rate.

Operation Concurrent

Indexing and control will be concurrent with arithmetic operations.

Except for arithmetic or Boolean compare instructions, the test overflow instructions with  $P_{33} = 1$ , or any arithmetic order that stores in any index register or stores in the location of the next instruction, the machine always gets its next instruction from the memory while it is doing the previous instruction. If this next instruction is one of the control and indexing orders, it is immediately done, unless it is an input-output order or a test overflow order. If it is done, it proceeds to get another instruction and do it, if possible. Thus almost all of the control and indexing orders can be done concurrently with the arithmetic or logical orders. Only the arithmetic and logical orders require the use of the main arithmetic unit of the machine.

All types of input-output orders can be done concurrently with other instructions. Automatic interlocks are provided so as to prevent timing conflict. Reference to a main memory position within the range of either an input or output instruction will halt the computer until the input or output transfer has occurred at that memory position. The computer is released as soon as the transfer of that particular word has been made and does not wait for the entire transfer to be completed. There is no interlock on the index memory when it is used as index registers. Only the effective addresses alpha, beta, and gamma are conflict checked. The programmer can easily make the computer wait until such a transfer is complete by using the last address in the index range of the input order in the A, B, or C addresses of a dummy order. An input-output instruction is not started until the previous arithmetic instruction is finished, hence the last arithmetic result may be included in the range of any input-output order.

As many as five input-output orders can be operating concurrently with computing and with each other. There is a separate trunk for reading cards, punching cards, using drum, and two separate trunks for using magnetic tape and all five of these trunks can operate concurrently.

## STORAGE

Media	No. of Words	Digits per Word	Access Microsec
Magnetic Core (Main)	4,096	72 binary	2
Magnetic Core (Index)	63	16 binary	1
Magnetic Drums (Two)	24,576		
Magnetic Tapes (Six)			
No. of units that can be connected		16 Units	
No. of chars/linear inch		400 Char/in	
Channels or tracks on the tape		16 Tracks/tape	
Blank tape separating each record		0.80 Inches	
Tape speed		150 Inches/sec	
Transfer rate	120,000	Char/sec	
Start time		3.0 Millisec	
Stop time		3.0 Millisec	
Average time for experienced operator to change reel		60 Seconds	

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Physical properties of tape

Width	1.0 Inch
Length of reel	2,500 Feet
Composition	0.43 Magnetic coating 1.45 Mil

Provision is made for up to 16,384 words of high speed memory and system can be expanded to 28 tape stations.

## INPUT

Media	Speed
Card Reader	800 cards/min
Magnetic Tape	See "Storage"

## OUTPUT

Media	Speed
Card Punch	250 cards/min
Magnetic Tape	See "Storage"

## Peripheral equipment

A single unit that is capable of converting alphanumeric characters from cards to tape, tape to high speed printer, tape to cards, cards to high speed printer and paper to magnetic tape.

## CIRCUIT ELEMENTS OF ENTIRE SYSTEM

Type	Quantity
Tubes	
5847	5,600
6197	110
6C4	110
6AQ5	220
Misc	80
Diodes	
LD70/CTP309	12,600
LD71	100,000
Misc	13,700
Transistors	
2N697	600
2N1143	240
2N398	1,600
Misc	6,300

## CHECKING FEATURES

Code checking features will include stopping on any selected address, the display of the contents of any memory cell, the display of normal or abnormal conditions, the ability to manually store in any

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selected memory cell, and the ability to transfer control to any part of the system. Parity checking is performed in each of the four 17-bit groups in each word.

## **POWER, SPACE, WEIGHT, AND SITE PREPARATION**

Power, computing system	35 Kw
Power, air conditioner	20 Kw
Space, computing system	Plenum is 30 ft x 40 ft
Space, air conditioner	(see below)
Capacity, air conditioner	25 Tons

Chilled water is sent two flights up to computer site to heat exchanger, transferring heat from computer closed loop air to closed loop chilled water. On ground floor, compressor refrigerant absorbs heat from chilled water. An evaporative system absorbs heat from refrigerant in a cooling tower. Compressor located two floors below. Liquid coolant piped upstairs. Heat exchanger, computer closed-loop air-to-coolant at computer site, and coolant-to-outside air downstairs.

## **PRODUCTION RECORD**

Number of systems produced to date            1  
Operational date anticipated as 1 April 1961.

## **COST, PRICE, AND RENTAL RATES**

The approximate cost, including an additional bank of 4,096 words of high speed memory, 6 tape stations, the system as described, with all peripheral converters and input-output equipment, site preparation, overhead and other related costs will be approximately 2.0 million dollars.

## **PERSONNEL REQUIREMENTS**

	Three 8-Hour Shifts
Supervisors	6
Analysts	3
Programmers and Coders	14
Clerks	1
Engineers	1
Technicians	6

No engineers are assigned to the operation of the machine, but are used for development and design of additions to the machine. The technicians consult the engineers when a total break-down occurs.

## **RELIABILITY, OPERATING EXPERIENCE, AND TIME AVAILABILITY**

A high degree of reliability is achieved by utilizing standard logical plug-in packages, a ruggedized, long life, driver tube, derated components and point-to-point soldered connections.

## **INSTALLATIONS**

Computing Laboratory  
Ballistic Research Laboratories  
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**APPENDIX V -- Inventory of Computers Within the U.S. Army  
Ordnance Corps - FY 1961**

ORGANIZATION	QUAN.	COMPUTERS	APPLICATION	OPERATING COST P/A IN KILO	PERSONNEL
Anniston Ord. Dep.	1	IBM 650	Supply	854	90
	1	IBM 1401	Management		
Benicia Arsenal	2	IBM 305	Supply	1,068	106
			Management		
Erie Ord. Dep.	2	IBM 305	Supply	894	93
			Management		
Letterkenny Ord. Dep.	2	IBM 305	Supply	1,271	120
			Management		
Mt. Ranier Ord. Dep.	2	IBM 305	Supply	709	73
			Management		
Pueblo Ord. Dep.	2	IBM 305	Supply	1,057	113
			Management		
Raritan Arsenal	2	IBM 305	Supply	1,889	39
	1	RCA 501	Management		
Red River Arsenal	2	IBM 305	Stock	950	113.6
			Management		
Rossford Ord. Dep.	1	IBM 1401	Supply	574	74
			Management		
Los Angeles Ord. Dep.	1	IBM 305	Supply	124	12
			Management		

ORGANIZATION	QUAN.	COMPUTERS	APPLICATION	OPERATING COST P/A IN KILO	PERSONNEL
WSMR	1	Univac 1103 A	Sci. Engin.		
	1	Burroughs E 101	Sci. Engin.		
	1	Bendix	Sci. Engin.		
	1	USS 80	Sci. Engin.		
	1	IBM 7090	Sci. Engin.		
	1	IBM 1401	Fin. Acct.		
			Pers. Manag.		
	1	Burroughs E101	Sci. Engin.		
	3	IBM 610	Sci. Engin.		
	1	IBM 704	Sci. Engin.		
	3	IBM 1620	Sci. Engin.		
	1	IBM 1401	Sci. Engin.		

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	1	IGP-30	Sci. Engin.		
	1	Bendix G-15	Sci. Engin.	3,563	118
Frankford Arsenal	1	IBM 650	Sup. Manag.		
	1	IBM 1401	Sup. Manag.		
	1	IBM 305	Fin. Acct.		
	1	Univac			
		File (D)	Sup. Manag.		
	1	Bendix G-15	Opt. Ray Tracing Ammunition		
	1	LGP 30	Opt. Design Studies		
	1	NCR 102 D	Weapons Studies		
	1	USS 90	Weapons Studies	1,574	118
<b>ORGANIZATION</b>	<b>QUAN.</b>	<b>COMPUTERS</b>	<b>APPLICATION</b>	<b>OPERATING COST P/A IN KILO</b>	<b>PERSONNEL</b>
Army Rocket Guided Missile Agency	1	Burroughs 205	Sci. Engin.		
	1	Elecom	Sci. Engin.		
	1	IBM 610	Sci. Engin.		
	1	IBM 1620	Sci. Engin.	913	116
Ordnance Tank-Automotive Command	1	RCA BIZMAC	Sup. Manag.		
	1	RCA 503	Sup. Manag.		
	1	RCA 501	Financial Acct.	2,706	318
Detroit Arsenal	1	Burroughs 204	Tank Automotive Research	100	6.5
Ordnance Ammunition Command	1	RCA 501	Special Weapons and Ammunition	419	32
Picatinny Arsenal	1	IBM 650	Engineering R and D		
	1	IBM 709	Ammunition Research		
	1	IBM 1401	Ammunition Research		
	1	IBM 502	Fin. and Personnel	655	19.5
Ordnance Weapons Command	1	RCA 501	Sup. Manag.	983	74
<b>ORGANIZATION</b>	<b>QUAN.</b>	<b>COMPUTERS</b>	<b>APPLICATION</b>	<b>OPERATING COST P/A IN KILO</b>	<b>PERSONNEL</b>

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APG	1	Bendix	Analysis of		
		G-15	Test Data		
	1	Burroughs	Analysis of		
		E-101	Test Data		
	1	ORDVAC	Sci. Research		
	1	BRLESC	Sci. Research		
	1	EDVAC	Sci. Research	771	76
Army Ord. Missile Command-Hq.	1	LGP-30	Classified	4	0
Army Ballistic Missile Agency (Now NASA Eff. 1 Jul 60)	1	IBM 704	Sci. Engin.		
	1	IBM 709	Sci. Engin.		
	1	IBM 7090	Sci. Engin.		
	2	IBM 714	Sci. Engin.		
	2	IBM 720	Sci. Engin.		
	2	IBM 730	Sci. Engin.		
	4	IBM 610	Sci. Engin.		
		M-2			
	1	IBM 705	Sup. Manag.		
	6	Burroughs	Sci. Engin.		
		205 (C)			
	10	LGP-30	Sci. Engin.		
	1	Bendix	Sci. Engin.		9
		G-15D			
Army Ballistic Missile Agency	3	LGP-30	Sci. Engin.		
	6	IBM 1620	Sci. Engin.		
	2	CDC 160	Data Reduction		
Redstone Arsenal	1	IBM 1401	Financial Acct.	781	60
ORGANIZATION	QUAN.	COMPUTERS	APPLICATION	OPERATING COST P/A IN KILO	PERSONNEL
Watervliet Arsenal	1	IBM 650	Engin. and Fiscal	195	20
Watertown Arsenal	1	RCA 501	Fin. and Personnel		
	1	LGP 20	Sci. Engin.		
	1	LGP 30	Sci. Engin.	365	40
Springfield Armory	1	NCR 304	Fin. and Personnel	44	6

NOTE: This is a complete list of all electronic digital systems, for all purposes, in use by U.S. Army Ordnance Corps. The list was taken from the report submitted by the Chief of Ordnance to the Department of the Army.

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**APPENDIX VI -- Arithmetic Operation Time (Including Access)  
of Computing Systems**

ADD TIME MICROSECONDS	MULTIPLY TIME MICROSECONDS	DIVIDE TIME MICROSECONDS	SYSTEM
2.5-27.5	14-61.5	5-63.5	AN/FSQ 31 (v)
2.5-27.5	14-61.5	56.5-70	AN/FSQ 32
3	20	40	WESTINGHOUSE AIRBORNE
3.7-11.7	42.3-50.3	45-53.0	PHILCO 2000
4	26	46	LITTON C 7000
4	12.7	31	UNIVAC 1107
4	8	28	UNIVAC LARC
4.36-32.70	4.36-30.52	6.54-32.70	IBM 7090
4.8	9.6 to 19.2	19.6 to 80.0	LINCOLN TX 2
4.8-9.6	25.2 to 0.8N	63.6-66.4	CDC 1604
5	65	80	BURROUGHS D 103
5	300	600	PROGRAMMED DATA PROCESSOR
5	10	105	SYLVANIA UDOFIT
5-6	25	65	BRLESC
6	1,000	1,000	LINCOLN TX 0
6.4-19.2	-	-	CDC 160
7-16	108	108	OKLAHOMA UNIVERSITY
7.2-12	19.2-84	84	UNIVAC 490
8	140	330	MERLIN
8	43	44	SYLVANIA S 9400
9	76.5-184.5	76.5-312.5	UNIVAC III
9.75	13.75	28.75	RCA 601
10	40	80	BURROUGHS D 202
10	56	70	IBM 7074
10	25	45	TARGET INTERCEPT
10	-	-	TRICE
10.2-12.6	30-108	108	BURROUGHS D 204
12.0	16.5	51.0	AN/FSQ 7 AN/FSQ 8 (SAGE)
12	60-102	60-102	LITTON DATA ASSESSOR
13.08 (6+6)	140 (6x6)	210 (10/6)	IBM 7080
16	35.2-112	112	AN/USQ 20
16	-	-	ITT SPES 025
16	86	88	MOBIDIC A
16	86	88	MOBIDIC C D & 7A
17 Digit	-	-	IBM 705 I II
20	-	-	CUBIC TRACKER
20.7	392	425	AN/TYK 7v INFORMER
22	300-600	575-725	NAREC
22	-	-	STORED PROGRAM DDA
22	34-41	71	WHIRLWIND II
22-26	238-242	238-242	AN/TYK 6v BASICPAC

TABLE V (CONTINUED)

Arithmetic Operation Time (Including Access) of Computing Systems

**ELECTRONIC COMPUTERS WITHIN THE ORDNANCE CORPS  
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ADD TIME MICROSECONDS	MULTIPLY TIME MICROSECONDS	DIVIDE TIME MICROSECONDS	SYSTEM
24	264	288	AN/SQ 28 (v) MDC
24	252	252	COMPAC
24	162	450	HONEYWELL 800
24	84	84	LINCOLN CG 24
24	96	168	RCA 300
24+n/2	71	81	MANIAC III
24-84	24-240	36-240	IBM 704
24-84	24-240	36-240	IBM 709
25	75	75	BURROUGHS D 201
25	75	-	CCC REAL TIME
25	400	400	JOHNNIAC
26	700	750	BURROUGHS D 208
27	70	112	BENDIX G 20
32	-	-	BURROUGHS D 209
32	366	380	LIBRASCOPE AIR TRAFFIC
32	-	-	MODAC 5014
33	-	-	NORDEN VOTE TALLY
36	80	128	RW 400
36 or 60	456	456	IBM 701
40	230	426	BURROUGHS D 107
40	250	500	GENERAL ELECTRIC 225
40	375	520	LEPRECHAUN
40	40 to 424	40 to 460	LIBRASCOPE MK 130
42	88	-	MOBIDIC B
42	294	1,044	NATIONAL 315
44	239	486	UNIVAC 1103 1103 A
45	-	-	PHILCO CXPQ
50	85	85	RICE UNIVERSITY
50 to 140	-	-	INTELEX AIRLINE RESERVATION
56	728	868	RCA 110
59	59	177	LIBRASCOPE CP 209
60	116	508	UNIVAC 1105
64	550	1,200	GENERAL ELECTRIC 210
64	368	-	SWAC
70	370-590	590	ORACLE
72 (10+10)	672 to 1,488 (10x10)	792 to 984	IBM 7070
80	840	940	GENERAL MILLS AD/ECS
84	84+84/Bit	84+84/Bit	HUGHES LRI X
86	3,000	3,000	BURROUGHS D 203
90	300-1,700	-	AF/CRC
93	665-865	950	ILLIAC

TABLE V (CONTINUED)

Arithmetic Operation Time (Including Access) of Computing Systems

ADD TIME MICROSECONDS	MULTIPLY TIME MICROSECONDS	DIVIDE TIME MICROSECONDS	SYSTEM
95.8	770.8	3,159.2	IBM 705 III

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100	990	1,200	CYCLONE
100	1,000	1,100	MISTIC
108	372	348	PACKARD BELL 250
120	1,520	16,200	GENERAL MILLS APSAC
120	540	540	MONROBOT V
120	1,320	3,480	NATIONAL 304
160	1,720	3,030	UNIVAC II
160	-	-	VERDAN
170	680-10,710	-	ITT BANK LN PROC
176-264	4,000	6,000	UDEC I II III
192	2,016	2,592	GENERAL ELECTRIC 312
160+16 (Aug+Add)	80+16	80+16	TELEREGISTER TELEFILE
192-1,536	2,208-3,552	2,256-3,600	EDVAC
192-1,536	2,304-3,648	2,304-3,648	DYSEAC
192-1,540	2,300-3,650	2,300-3,650	SEAC
200	2,070	3,985	BURROUGHS 220
200	860	1,420	HONEYWELL 290
210	105+105/Bit	105/Bit	HUGHES DIGITAIR
210	7,800	-	RCA 301
220	1,760	5,300	HAMPSHIRE TRTDS 932
221	-	-	SPEC
224	13,860 (6x6)	17,640 (6/6)	IBM 609
230.4	1,008	2,304	DATAMATIC 1000
250	250	-	CUBIC AIR TRAFFIC
264	1,144	2,112	HUGHES M 252
300	1,960	2,170	IBM 1401
312	2,028	-	ASC 15
400-17,000	10,000-26,000	10,000-26,000	OARAC
428	8,500	8,000	HAMPSHIRE CCC 500
440	25,000	40,000	READIX
500	500-1,000	-	LOGISTICS
500	17,000	17,000	RPC 4000
525	2,150	3,950	UNIVAC I
540	2,430-16,700	2,430-16,700	BENDIX G 15
540	10,800	11,300	RECOMP II
560	3,137	4,830	DIANA
624	3,744	3,744	AN/ASQ 28 (v) EDC
625	4,219	4,375	LIBRASCOPE ASN 24
780	2,990	3,120	RW 300
910	3,600	3,600	LEEDS NORTHROP 3000

TABLE V (CONTINUED)

Arithmetic Operation Time (Including Access) of Computing Systems

ADD TIME MICROSECONDS	MULTIPLY TIME MICROSECONDS	DIVIDE TIME MICROSECONDS	SYSTEM
924	4,224	4,224	PHILCO 3000
960 (10 Dig)	17,700 (10 Dig)	16.8	IBM 1620
1,000	17,000	17,000	ALWAC III E
1,000	17,000	17,000	LIBRATROL 1000
1,019-1,188	9,300	12,680	BURROUGHS 204
1,019-1,188	9,300	12,680	BURROUGHS 205

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1,110	2,860	3,520	RPC 9000
1,360	1,275	1,275	UNIVAC SOLID STATE 80/90
1,360	1,275 +	1,275 +	UNIVAC STEP
1,980	22,240	22,740	REPAC
2,000	21,000	21,500	RECOMP I CP 266
3,445	5,335	7,426	PENNSTAC
3,500	22,000	22,000	ELECOM 125 125FP
7,750	23,000	23,000	LIBRATROL 500
7,800	21,000 to 49,100	21,000 to 53,200	NATIONAL 102 D
8,000	17,000	17,000	LGP 30
8,000	8,000	8,000	MODAC 414
8,000	68,000	77,000	MONROBOT MU
8,700	23,800	27,500	UNIVAC FILE 0
8,700	23,800	27,500	UNIVAC FILE 1
9,000	34,000	500,000	MONROBOT XI
9,590	19,850	20,390	JUKEBOX
11,000	250,000	400,000	NATIONAL 390
11,200	24,300	25,600	MINIAC II
12,000	13,500	54,000	MONROBOT IX
15,000	40,000	40,000	NATIONAL 107
16,700	16,700	16,700	WISC
17,010	-	-	TELEREGISTER UNIFIED AIRLINES
19,900	37,500	38,500	NATIONAL 102 A
20,000	-	-	ELECOM 100
25,000	-	-	MODAC 404
30,000	60,000-190,000	100,000-370,000	IBM 305 RAMAC
50,000	250,000	250,000	BURROUGHS E 101
50,000	250,000	250,000	BURROUGHS E 102
51,000	250,000	300,000	BURROUGHS E 103
60,000	220,000	200,000	DE 60
110,000	2,500,000	-	IBM 632
120,000	540,000	540,000	MONROBOT III
135,000	600,000	600,000	MONROBOT VI

**APPENDIX VII -- Approximate Cost of Computing Systems**

TABLE XIV

Approximate Cost of Computing Systems  
(Basic or Typical System)

COST	SYSTEM	COST	SYSTEM
\$ 1,000	PERK I II	\$ 86,074	MONROBOT V
6,000	IBM 632	87,500	RPC 4000
9,650	MONROBOT IX	95,000	RECOMP II
15,000	HRB SINGER	97,000	ELECOM 120
17,000 to 20,000	ITT BANK LN PROC	97,500	UNIVAC 120
18,000	DE 60	98,000	RW 300
19,195	SPEC	100,000	MODAC 404
20,000	GEOTECH AUTOMATIC	100,000	PENNSTAC

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20,000	MAGNEFILE B	110,000	PROGRAMMED DATA PROCESSOR
22,500	ELECOM 50	120,000	MODAC 410
24,500	MONROBOT XI	120,000	RPC 9000
29,750	BURROUGHS E 101	125,600	IBM 1401
29,750	BURROUGHS E 102	127,000	FOSDIC
29,750	BURROUGHS E 103	141,980	GENERAL MILLS AD/ECS
36,000	IBM 609	150,000	MODAC 414
40,500	PACKARD BELL 250	155,000	ELECOM 125 125FP
45,000	DISTRIBUTAPE	160,000	BURROUGHS D 204
49,500	BENDIX G 15	167,850	IBM 305 RAMAC
49,500	LPG 30	170,000	HONEYWELL 290
50,000	ALWAC II	175,000	UNIVAC STEP
50,000	HAMPSHIRE CCC 500	182,000	IBM 650 RAMAC TAPES
50,000	MAGNEFILE D	185,000	OARAC
50,000	TRICE	196,000	RCA 301
50,000 to 100,000	HAMPSHIRE TRTDS 932	200,000	BURROUGHS 204
55,000	BENDIX D 12	200,000	BURROUGHS 205
55,000	IBM 610	200,000	GENERAL ELECTRIC 225
56,300	NATIONAL 390	200,000	RASTAC
60,000	CDC 160	200,000	RASTAD
60,000	ELECOM 100	225,000	GENERAL ELECTRIC 210
64,000	IBM 1620	225,000	NUMERICORD
65,000	NATIONAL 102 D	230,000	IBM 701
70,000	NATIONAL 102 A	250,000	MANIAC I
70,000	READIX	257,000	RCA 501
75,000	IBM CPC	300,000	ILLIAC
75,000	UNIVAC 60	300,000	TELEREGISTER MAGNET INVENT CONT
76,950	ALWAC III E	300,000	UNIVAC FILE 1
80,000	AN/MJQ 1 REDSTONE	300,000	UNIVAC FILE 0
80,000	CIRCLE	320,000	BURROUGHS 220
82,500	NATIONAL 315	347,500	UNIVAC SOLID STATE 80/90
84,500	LIBRATROL 500	350,000	MANIAC II
85,000	MINIAC II	350,000	UNIVERSAL DATA TRANS
85,000	MODAC 5014	354,000	LOGISTICS
85,200	GENERAL ELECTRIC 312	358,000	IBM 702

TABLE XIV (CONTINUED)

Approximate Cost of Computing Systems  
(Basic or Typical System)

COST	SYSTEM
\$ 366,600	NATIONAL 304
400,000	RICE UNIVERSITY
400,000	SWAC
467,000	EDVAC
478,000	BENDIX G 20
500,000	AN/TYK 6v BASICPAC
500,000	GEORGE
500,000	UDEC I II III
500,000 (Donated)	UNIVAC 1101
600,000	MERLIN

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600,000		NORDEN VOTE TALLY
600,000		ORDVAC
700,000		UNIVAC III
750,000		CDC 1604
750,000		UNIVAC I
800,000		AF/CRC
813,250		IBM 7070
839,700		RCA 601
895,000		UNIVAC 1103 1103A
970,000		UNIVAC II
975,000		HONEYWELL 800
1,000,000		ITT SPES 025
1,000,000		LINCOLN CG 24
1,000,000		NATIONAL 107
1,284,350		IBM 7074
1,400,000		UNIVAC 1102
1,500,000		NAREC
1,500,000		UNIVAC 490
1,600,000		PHILCO CXPQ
1,640,000		IBM 705 I II
1,800,000	to 2,700,000	UNIVAC 1107
1,932,000		UNIVAC 1105
1,994,000	(Excluding Discount)	IBM 704
2,000,000		BRLESC
2,179,100		DATAMATIC 1000
2,200,000		IBM 7080
2,500,000		NORC
2,630,000		IBM 709
2,898,000		IBM 7090
4,500,000		BIZMAC I
6,000,000		UNIVAC LARC

## APPENDIX VIII -- Glossary

Glossary of Computer Engineering and Programming Terminology  
(Partial list from BRL Report 1115, March 1961)

### ACCESS, RANDOM

Access to storage under conditions in which the next position from which information is to be obtained is in no way dependent on the previous one.

### ACCESS TIME

(1) The time interval between the instant at which information is: (a) called for from storage and the instant at which delivery is completed, i.e., the read time; or (b) ready for storage and the instant at which storage is completed, i.e., the write time. (2) the latency plus the word-time.

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**ACCURACY**

Freedom from error. Accuracy contrasts with precision; e.g., a four- place table, correctly computed, is accurate; a six-place table containing an error is more precise, but not accurate.

**ADDER**

A device capable of forming the sum of two or more quantities.

**ADDRESS**

A label such as an integer or other set of characters which identifies a register, location of device in which information is stored.

**ANALOG**

The representation of numerical quantities by means of physical variables, e.g., translation, rotation, voltage, resistance; contrasted with "digital."

**ANALYZER, DIFFERENTIAL**

An analog computer designed and used primarily for solving many types of differential equations.

**AND-OPERATOR**

A logical operator which has the property such that if P and Q are two statements, then the statement "P and Q" is true or false precisely according to the following table of possible combinations:

P		Q		P and Q	
False	0	False	0	False	0
False	0	True	1	False	0
True	1	False	0	False	0
True	1	True	1	True	1

The "and" operator is often represented by a centered dot (.), or by no sign, as in P. Q or PQ; the term conjunction is applied to this operator.

**AND-GATE**

A signal circuit with two or more input wires which has the property that the output wire gives a signal if and only if all input wires receive coincident signals. ARITHMETIC UNIT That portion of the "hardware" of an automatic computer in which the arithmetic and logical operations are performed.

**AUTOMATION**

The entire field of investigation, design, development, application, and methods of rendering or making processes or machines self-acting or self- moving; rendering automatic; theory, art or

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technique of making a device, machine, process or procedure more fully automatic; the implementation of a self-acting or self-moving, hence, automatic process or machine.

## **BINARY**

A characteristic or property involving a selection, choice or condition in which there are but two possible alternatives.

## **BINARY, NUMBER**

A single digit or group of characters or symbols representing the total, aggregate or amount of units utilizing the base two; usually using only the digits "0" and "1" to express quantity.

## **CAPACITY**

The upper and lower limits of the numbers which may be processed in a computer register, e.g., in the accumulator, e.g., the capacity of a computer may be ten decimal digits or the capacity of a computer may be +.00000 00001 to +.99999 99999. Quantities which exceed the capacity usually interrupt the operation of the computer in some fashion; the quantity of information which may be stored in a storage unit; see Capacity, Storage.

## **CAPACITY, STORAGE**

Maximum number of words or characters which a device is capable of storing; a measure of the ability of a device to store information for future reference.

## **CHARACTER**

One of a set of elementary symbols such as those corresponding to the keys on a typewriter. The symbols usually include the decimal digits 0 through 9, the letters A through Z, punctuation marks, operation symbols, and any other single symbols which a computer may read, store, or write; a pulse code representation of such a symbol.

## **CHECK**

A means of verification of information or operation during or after an operation.

## **CODE**

A system of symbols or their use in representing rules for handling the flow or processing of information; to actually prepare problems for solution on a specific computer.

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## **CODING**

The list, in computer code or in pseudo-code, of the successive computer operations required to solve a given problem; repertoire of instructions. CODING, ALPHABETIC A system of abbreviation used in preparing information for input into a computer such that information is reported in the form of letters, e.g., New York as NY, carriage return as CN, etc.

## **CODING, AUTOMATIC**

Any technique in which a computer is used to help bridge the gap between some "easiest" form, intellectually and manually, of describing the steps to be followed in solving a given problem and some "most efficient" final coding of the same problem for a given computer; two basic forms are Routine, Compilation and Routine, interpretation.

## **CODING, NUMERIC**

A system of abbreviation used in the preparation of information for machine acceptance by reducing all information to numerical quantities; in contrast to alphabetic coding.

## **COMMAND**

A pulse, signal, or set of signals initiating one step in the performance of a computer operation; that portion of the instruction word which specifies the operation to be performed; see instruction.

## **COMPUTER**

Any device capable of accepting information, applying prescribed processes to the information, and supplying the results of these processes; sometimes, more specifically, a device for performing sequences of arithmetic and logical operations; sometimes, still more specifically, a stored-program digital computer capable of performing sequences of internally-stored instructions, as opposed to calculators on which the sequence is impressed manually (desk calculator) or from tape or cards (card programmed calculator).

## **COMPUTER, ANALOG**

A calculating machine which solves problems by translating physical conditions like flow, temperature or pressure into electrical quantities and using electrical equivalent circuits for the physical phenomenon.

## **COMPUTER, ASYNCHRONOUS**

A calculating device in which an operation is initiated by a signal generated upon completion of a previous operation; contrasted with Synchronous Computer.

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## **COMPUTER, AUTOMATIC**

A calculating device which handles long sequences of operations without human intervention.

## **COMPUTER, DIGITAL**

A calculating device utilizing numbers to express all the variables and quantities of a problem. The numbers are usually expressed as a space-time distribution of punched holes, electrical pulses, sonic pulses, etc.

## **COMPUTER, SYNCHRONOUS**

A calculating device in which the performance of all operations is controlled with periodic signals from a master clock.

## **CONTROL**

(1) Usually, those parts of a digital computer which effect the carrying out of instructions in proper sequence, the interpretation of each instruction, and the application of the proper signals to the arithmetic unit and other parts in accordance with this interpretation. (2) Frequently, one or more of the components in any mechanism responsible for interpreting and carrying out manually-initiated directions. Sometimes called manual control. (3) In some applications of mathematics, a mathematical check.

## **CONTROL-UNIT**

That portion of the hardware of an automatic digital computer which directs the sequence of operations, interprets the coded instructions, and initiates the proper commands to the computer circuits to execute the instructions.

## **CORE, MAGNETIC**

A magnetic material capable of assuming and remaining at one of two or more conditions of magnetization, thus capable of providing storage, gating or switching functions, usually of toroidal shape and pulsed or polarized by electric currents carried on wire adjacent the material.

## **DATA-REDUCTION**

The art or process of transforming masses of raw test or experimentally obtained data, usually gathered by instrumentation, into useful, ordered, or simplified intelligence.

## **DECODE**

To ascertain the intended meaning of the individual characters or groups of characters in the pseudo-coded program.

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## **DIGIT**

One of the  $n$  symbols of integral value ranging from 0 to  $n-1$  inclusive in a scale of numbering of base  $n$ , e.g., one of the ten decimal digits, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.

## **DIGIT, BINARY**

A whole number in the binary scale of notation; this digit may be only 0 (zero) or 1 (one). It may be equivalent to an "on" or "off" condition, a "yes" or a "no," etc.

## **DIGITAL**

The quality of utilizing numbers in a given scale of notation to represent all the quantities that occur in a problem or a calculation.

## **DOWN-TIME**

The period during which a computer is malfunctioning or not operating correctly due to machine failures; contrasted with available time, idle time or standby time. Scheduled maintenance time is also considered down-time, in as much as the computer is unable to operate during this period.

## **DRUM, MAGNETIC**

A rotating cylinder on whose magnetic-material coating information is stored in the form of magnetized dipoles, the orientation or polarity of which is used to store binary information.

## **ELECTRONIC**

Pertaining to the application of that branch of science which deals with the motion, emission, and behavior of currents of free electrons, especially in vacuum, gas or phototubes and special conductors or semi-conductors. Contrasted with electric which pertains to the flow of large currents in wires or conventional conductors.

## **ERROR**

The amount of loss of precision in a quantity; the difference between an accurate quantity and its calculated approximation; errors occur in numerical methods, e.g., an error introduced by the truncation of a power series defining a transcendental function. This may be classified as an error introduced by the numerical method, there is no mistake involved and the computer is operating properly; mistakes occur in programming, coding, data transcription, and operating, thus, usually humans make mistakes, e.g., assigning a wrong address when coding a problem; malfunctions occur in computers and are due to physical limitations on the properties of materials. An error is sometimes considered to be the differential margin by which a controlled unit deviates from its target value.

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## FLIP-FLOP

A bi-stable device; a device capable of assuming two stable states; a bi-stable device which may assume a given stable state depending upon the pulse history of one or more input points and having one or more output points. The device is capable of storing a bit of information; a control device for opening or closing gates; a toggle.

## FUNCTION-TABLE

Two or more sets of information so arranged that an entry in one set selects one or more entries in the remaining sets; a dictionary; a device constructed of hardware, or a subroutine, which can either (a) decode multiple inputs into a single output or (b) encode a single input into multiple outputs; a tabulation of the values of a function for a set of values of the variable.

## GATE

A circuit which has the ability to produce an output which is dependent upon a specified type of or the co-occurrence nature of the input, e.g., an "and" gate has an output pulse when there is time coincidence at all inputs; an "or" gate has an output when any one or any combination of input pulses occur in time coincidence; any gate may contain a number of "inhibits," in which there is no output under any condition of input if there is time coincidence of an inhibit or "except" signal.

## HALF-ADDER

A circuit having two output points, S and C, and two input points, A and B, such that the output is related to the input according to the following table:

INPUT		OUTPUT	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

If A and B are arbitrary input pulses, and S and C are "sum without carry" and carry, respectively, it may be seen that two half-adders, properly connected may be used for performing binary addition.

## HARDWARE

The mechanical, magnetic, electronic, and electrical devices from which a computer is fabricated; the assembly of material forming a computer or component thereof.

## INFORMATION

An aggregation of data.

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## **INSTRUCTION**

A set of characters which defines an operation together with one or more addresses (or no address) and which, as a unit, causes the computer to operate accordingly on the indicated quantities. The term "instruction" is preferable to the terms "command" and "order;" command is reserved for electronic signals; order is reserved for "the order of the characters" (implying sequence) or "the order of the interpolation," or "the order of the differential equation."

## **LANGUAGE, MACHINE**

Expressions which define the operations of a computer, usually intelligible to the computer by means of its circuitry. It may be information recorded in a form which may be made available to a computer; coded information which can be sensed by a machine.

## **LOGIC**

The science that deals with the canons and criteria of validity in thought and demonstration; the science of the formal principles of reasoning; the basic principles and applications of truth tables, gating, interconnection, etc. required for arithmetic computation in a computer.

## **MEMORY**

The term "storage" is preferred.

## **MICROSECOND**

A millionth part of a second. Abbreviated musec.

## **MILLISECOND**

A thousandth part of a second. Abbreviated msec.

## **MISTAKE**

A human blunder which results in an incorrect instruction in a program or in coding, an incorrect element of information, or an incorrect manual operation. See Error.

## **NUMBER, BINARY**

A numerical value written in the base-two system of notation. Usually the characters 0 and 1 are used to express numbers, although any pair of arbitrary symbols could be used.

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## OPERATION

A defined action; the action specified by a single computer instruction or pseudo-instruction; an arithmetical, logical, or transferal unit of a problem, usually executed under the direction of a subroutine.

## OPERATION, ARITHMETICAL

An operation in which numerical quantities form the elements of the calculation (e.g., addition, subtraction, multiplication, division).

## OPERATION, REAL-TIME or ON-LINE

The processing of data in synchronism or in coincidence with a physical process in such a fashion that the results of the data-processing are useful to the physical operation.

## OPERATION, SERIAL

The flow of information through a computer in time sequence, using only one digit, word, line or channel at a time. Contrasted with parallel operation.

## OR-OPERATOR

A logical operator which has the property such that if P or Q are two statements, then the statement "P or Q" is true or false precisely according to the following table of possible combinations:

P	Q	P or Q
False 0	True 1	True 1
True 1	False 0	True 1
True 1	True 1	True 1
False 0	False 0	False 0

The term disjunction is applied to this operator.

## OUTPUT

Information transferred from the internal storage of a computer to secondary or external storage; information transferred to any device exterior to the computer.

## PARALLEL

Handled simultaneously in separate facilities; operating on two or more parts of a word or item simultaneously; contrasted with serial.

## PLUG-BOARD

A removable panel containing an ordered array of terminals which may be interconnected by short electrical leads according to a prescribed pattern and hence designating a specific program or machine

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step. The entire panel, pre-wired, may be inserted for different programs. Used to a large extent in CPC's, printers, tabulators, summary punches and some computers e.g., the Univac File Computer.

## **PRECISION**

The degree of exactness with which a quantity is stated; a relative term often based on the number of significant digits in a measurement. See also Accuracy.

## **PROGRAMMER**

A person who prepares instruction sequences without necessarily converting them into the detailed codes of a particular computer. PUNCH, CARD A device which perforates or places holes in cards in specific locations designated by a program.

## **RANDOM-ACCESS**

Access to storage under conditions in which the next position from which information is to be obtained is in no way dependent on the previous one.

## **READ**

To copy, usually from one form of storage to another, particularly from external or secondary storage to internal storage; to sense the meaning or arrangements of hardware; to sense the presence of information on a recording medium.

## **READER, CARD**

A mechanism that permits the sensing of information punched on cards by means of wire brushes, metal feelers, or a photoelectric device, converting the information into electrical pulses that are sensible to the computing system.

## **READER, TAPE, MAGNETIC**

A device capable of restoring to a train or sequence of electrical pulses, information recorded on a magnetic tape in the form of a series of magnetized spots, usually for the purpose of transferring the information to some other storage medium.

## **READER, TAPE, PAPER**

A device capable of restoring to a train or sequence of electrical pulses, information punched on a paper tape in the form of a series of holes, usually for the purpose of transferring the information to some other storage medium.

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## **REAL-TIME**

The performance of a computation during the actual time that the related physical process transpires in order that results of the computations are useful in guiding the physical process.

## **ROUTINE**

A set of coded instructions arranged in proper sequence to direct the computer to perform a desired operation or series of operations.

## **RUN**

One performance of a program on a computer; performance of one routine, or several routines automatically linked so that they form an operating unit, during which manual manipulations are not required of the computer operator.

## **SCANNER**

An instrument which automatically samples or interrogates the state of various processes, conditions, or physical states and initiates action in accordance with the information obtained. SENSE To examine, particularly relative to a criterion; to determine the present arrangement of some element of hardware, especially a manually-set switch; to read holes punched in paper.

## **SEQUENCER**

A machine which puts items of information into a particular order, e.g., it will determine whether A is greater than, equal to, or less than B, and sort or order accordingly.

## **STORAGE**

Preferred to memory, any device into which units of information can be copied, which will hold this information, and from which the information can be obtained at a later time; devices, such as plugboards, which hold information in the form of arrangements of physical elements, hardware, or equipment; the erasable storage in any given computer.

## **STORAGE, MAGNETIC**

Any storage system which utilizes the magnetic properties of materials to store information.

## **STORAGE, MERCURY**

Columns of a liquid mercury medium used as a storage element by the delaying action or time of travel of sonic pulses which are circulated by having electrical amplifier, shaper, and timer circuits complete the loop.

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## **STORAGE, PARALLEL**

Storage in which all bits, or characters, or (especially) words are essentially equally available in space, without time being one of the coordinates. Parallel storage contrasts with serial storage. When words are in parallel, the storage is said to be parallel by words; when characters within words (or binary digits within words or characters) are dealt with simultaneously, not one after the other, the storage is parallel by characters (or parallel by bit respectively). Contrasted with Storage, Parallel.

## **STORAGE, SERIAL**

Storage in which time is one of the coordinates used to locate any given bit, character, or (especially) word. Storage in which words, within given groups of several words, appear one after the other in time sequence, and in which access time therefore includes a variable latency or waiting time of from zero to many-times, is said to be serial by word. Storage in which the individual bits comprising a word appear in time sequence is serial by bit. Storage for coded-decimal or other non-binary numbers in which the characters appear in time sequence is serial by character; e.g., magnetic drums are usually serial by word but may be serial by bit, or parallel by bit, or serial by character and parallel by bit etc.

## **SUBROUTINE**

The set of instructions necessary to direct the computer to carry out a well defined mathematical or logical operation; a subunit of a routine. A subroutine is often written in relative or symbolic coding even when the routine to which it belongs is not. **SYSTEM** An assembly of components united by some form of regulated interaction; an organized whole.

## **TABULATOR**

A machine which reads information from one medium, e.g., cards, paper tape, magnetic tape, etc. and produces lists, tables, and totals on separate forms or continuous paper.

## **TAPE, MAGNETIC**

A tape or ribbon of any material impregnated or coated with magnetic material on which information may be placed in the form of magnetically polarized spots.

## **TRANSISTOR**

An electronic device utilizing semi-conductor properties to control the flow of currents from one source in one circuit by currents from another circuit, e.g., a triod transistor permits the control of current in one circuit by the use of a smaller current in another circuit, with the transistor common to both circuits.

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## **TUBE, CATHODE-RAY**

An electronic vacuum tube containing a screen on which information may be stored by means of a multigrid modulated beam of electrons from the thermionic emitter, storage effected by means of charged or uncharged spots; a storage tube; a Williams tube; an oscilloscope tube; a picture tube.

## **WORD**

A set of characters which occupies one storage location and is treated by the computer circuits as a unit and transported as such. Ordinarily a word is treated by the control unit as an instruction, and by the arithmetic unit as a quantity. Word lengths are fixed or variable depending on the particular computer.

## **APPENDIX IX -- Bibliography**

The following sources were used in the preparation of this monograph. The commercial books (open literature) were used mainly for background information and study while the reports, manuals, interviews, and material prepared by BRL personnel were used directly to write the various chapters.

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2. Interview with Mr. Harold L. Sprinkle, Electronics Engineer, for data regarding problems with ENIAC.
3. Interview with Mr. William H. Swann, Electronics Repairman, regarding the Bell Relay Computer.
4. Interview with Mr. Chester Wallin, regarding EDVAC.
5. Interview with Mr. James Hallman, regarding ORDVAC.

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6. Interview with Mr. Martin H. Weik, Technical Staff Assisting regarding:
  - a. Computing Systems in general.
  - b. ENIAC
  - c. EDVAC
  - d. ORDVAC
  - e. BRLESC
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  - g. Suggestions during preparation of monograph.