

Disk Atbus Definition (DAD)
Working Draft of the
Committee for a Common Access Method (CAM)
Rev 1
Draft Proposed

Abstract: This standard defines mechanical, electrical, and functional requirements for attaching small computers employing an ATBus with intelligent rigid disk drives. In addition to documenting the defacto and baseline interface, this standard also defines a downward compatible SCSI pass through mode. With the physical protocol of the ATBus I/O, not all SCSI functionality is required. Consequently this standard includes a brief summary of SCSI functionality not included. The resulting interface provides a common interface specification for systems manufacturers, system integrators, controller manufacturers, and suppliers of intelligent disk drives.

WARNING: This is a preliminary draft of the proposed DAD standard. It is subject to change without notice, at the sole discretion of the CAM Group. It is likely that some sections may change significantly, and most sections will change to some extent in the course of further development of this draft standard. This draft is distributed solely for the purpose of review and comment, and it should not be used as a design document without assuming the risk of such an early implementation.

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6.0 SCSI PASS THROUGH MODE

7.0 SCSI RESTRICTIONS USING ATBUS PASS THROUGH MODE
DRAFT PROPOSED DISK ATBUS DEFINITION (DAD) 25 March 1989

4.0 INTERFACE CABLING REQUIREMENTS

4.1 GENERAL DESCRIPTION

This standard describes the interface requirements of a disk drive which is compatible with the Requirements of the "ATBus". Data is transferred in parallel (16 bits) from the Host bus to the drive's Buffer. Under direction of commands previously transferred from the Host. The drive's controller performs all of the operations necessary to properly write data on or read data from disk media. Data read from the media is stored in the Buffer and transferred to the Host.

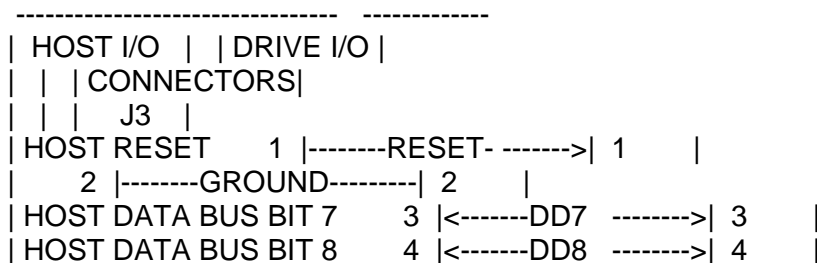
Section ?? of this standard describes how this interface is used, in a downward compatible manner to pass SCSI commands, data transfers, and status.

This standard provides the capability of operating on the AT bus in a daisy chained configuration with a second drive|controller that operates in accordance with these standard s. One drive is designated as master and the other as the slave (see Figure 4.1-1).

Selection of the Master drive is made by a jumper plug or switch.

4.2 PHYSICAL INTERFACE

The physical interface consists of single ended TTL compatible receivers and drivers communicating through a 40 conductor flat ribbon nonshielded cable with a maximum length 24 inches (0.61 metre) using asynchronous interface protocol. A diagram of the Host-drive interface showing pin numbers and signal names is shown in Figure 4.2-1. Detail descriptions of the signal functions are given in section 11 with interface timing protocol shown in the waveforms of Figures 5.2-1, 5.2-2 and 5.2-3. Details of the DC and Data cables and connectors are given in Sections 4.3 and 4.4.

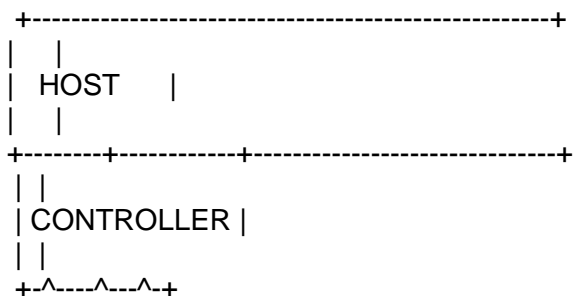


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HOST DATA BUS BIT 6	5	<-----DD6 ----->	5	
HOST DATA BUS BIT 9	6	<-----DD9 ----->	6	
HOST DATA BUS BIT 5	7	<-----DD5 ----->	7	
HOST DATA BUS BIT 10	8	<-----DD10 ----->	8	
HOST DATA BUS BIT 4	9	<-----DD4 ----->	9	
HOST DATA BUS BIT 11	10	<-----DD11 ----->	10	
HOST DATA BUS BIT 3	11	<-----DD3 ----->	11	
HOST DATA BUS BIT 12	12	<-----DD12 ----->	12	
HOST DATA BUS BIT 2	13	<-----DD2 ----->	13	
HOST DATA BUS BIT 13	14	<-----DD13 ----->	14	
HOST DATA BUS BIT 1	15	<-----DD1 ----->	15	
HOST DATA BUS BIT 14	16	<-----DD14 ----->	16	
HOST DATA BUS BIT 0	17	<-----DD0 ----->	17	
HOST DATA BUS BIT 15	18	<-----DD15 ----->	18	
	19	-----GROUND-----	19	
	20	------(KEYPIN)-----	20	
RESERVED	21	-----RSVD -----	21	
	22	-----GROUND-----	22	
HOST I/O WRITE	23	-----DIOW- ----->	23	
	24	-----GROUND-----	24	
HOST I/O READ	25	-----DIOR- ----->	25	
	26	-----GROUND-----	26	
RESERVED	27	-----RSVD -----	27	
HOST ADDRESS LATCH ENABLE	28	-----DALE ----->	28	
RESERVED	29	-----RSVD -----	29	
	30	-----GROUND-----	30	
HOST INTERRUPT REQUEST	31	<-----INTRQ -----	31	
HOST 16 BIT I/O	32	<-----IOCS16 -----	32	
HOST ADDRESS BUS	33	-----DA1 ----->	33	
PASSED DIAGNOSTICS	34	<-----PDIAG ----->	34	
HOST ADDRESS BUS	35	-----DAO ----->	35	
HOST ADDRESS BUS	36	-----DA2 ----->	36	
HOST CHIP SELECT 0	37	-----CS1FX- ----->	37	
HOST CHIP SELECT 1	38	-----CS3FX- ----->	38	
DRIVE ACTIVE SLAVE PRESENT	39	-----DASP- ----->	39	
	40	-----GROUND-----	40	
-----	-----			

FIGURE 4.2-1. HOST TO DISK DRIVE INTERFACE DIAGRAM



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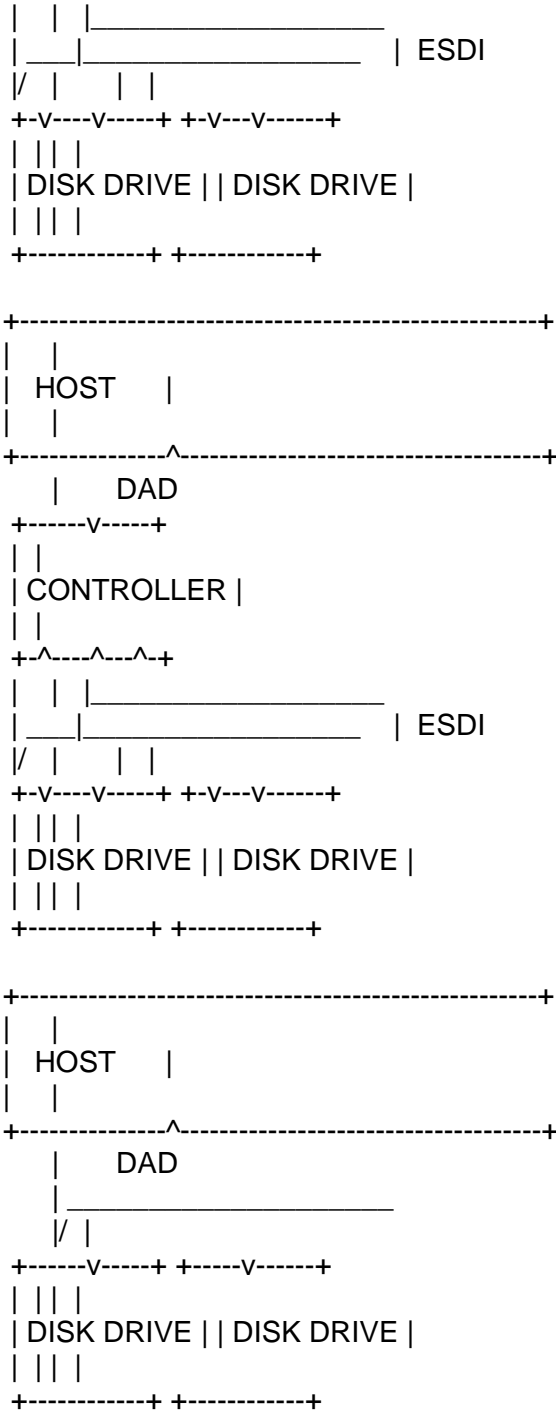


FIGURE 4.1-1. INTERFACE CABLING OPTIONS

4.3 DC CABLE AND CONNECTOR

The drive receives DC power through a 4 pin connector (see Table 4.3-1 for pin assignment). Recommended part numbers for the mating connector are included below, but equivalent parts may be used (See Table 4.3-2).

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Drive Connector Terminal Cable Connector Terminal

AMP P/N 61664-1 AMP P/N 62137-2

TABLE 4.3-1 DC INTERFACE

POWER LINE DESIGNATION		PIN NUMBER
+12 V	J1-01	
+12 V RETURN	J1-02	
+5 V RETURN	J1-03	
+5 V	J1-04	

TABLE 4.3-2. MATING PARTS

TYPE OF CABLE	CONNECTOR	CONTACTS
18 AWG	AMP 1-480424-0	AMP 60619-4
	(Loose Piece)	
	AMP 61117-4	
	(Strip)	

4.3.1 Device Grounding

Provision for tying the DC Logic ground and the chassis ground together or for separating these two ground planes is vendor specific.

4.4 I/O CABLE AND CONNECTOR

The I/O connector is a 40 pin connector (Figure 4.4-1). The odd pins are located along the edge of the printed circuit board with pin 1 leftmost. The even pins are on the side away from the edge of the printed circuit board. A key is provided by the removal of Pin 20. The corresponding pin on the cable connector should be plugged. The connector should be keyed to prevent the possibility of installing it upside down. See Figure 4.2-1 and Table 5.2-1 for a signal description summary.

The maximum cumulative I/O cable length shall be 24 inches (.61 metres).

Recommended part numbers for the mating connector are included below, but equivalent parts may be used.

CONNECTOR (40 PIN)

3M-3417-7000 (Strain relief 3448-2040)

CABLE

Flat Cable (Stranded AWG 28) 3M-3365-40

Flat Cable (Stranded AWG 28) 3M-3517-40 (Shielded Cable)

5.0 INTERFACE OPERATION AND REQUIREMENTS DESCRIPTION

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5.1 GENERAL

This section defines the details of the interface operation in the AT Bus compatible mode. See Sections 6 AND 7 for details of the SCSI pass through mode.

5.2 INTERFACE SIGNAL DESCRIPTIONS

5.2.1 Signal Conventions

Signal names are shown in all upper case letters. Signals can be asserted (active, true) in either a high (more positive voltage) or low (less positive voltage) state. A dash character (-) at the beginning or end of a signal name indicates it is asserted at the low level (active low). No dash or a plus character (+) at the beginning or end of a signal name indicates it is asserted high (active high). An asserted signal may be driven high or low by an active circuit, or it may be allowed to be pulled to the correct state by the bias circuitry. Control signals that are asserted for one function when high and asserted for another function when low are named with the asserted high function name followed by a slash character (/), and the asserted low function name followed with a dash (-). For example, BITENA/BITCLR- enables a bit when high and clears a bit when low. All signals are TTL compatible unless otherwise noted. Negated means that the signal is driven by an active circuit to the state opposite to the asserted state (inactive, or false) or may be simply released (in which case the bias circuitry pulls it inactive, or false), at the option of the implementor.

5.2.2 Signal Descriptions

Table 5.2-1 describes the interface signals and pins in more detail than given in Table 4.2-1. The signals are listed according to function, rather than in numerical connector pin order. The table lists signal name mnemonic, connector pin number, whether input to (I) or output from (O) the drive, signal full name and a brief signal description.

TABLE 5.2-1. INTERFACE SIGNAL DESCRIPTION SUMMARY

PIN NAME	PIN NUMBER	I/O	SIGNAL NAME	SIGNAL DESCRIPTION
RESET-	1	I	Drive reset	Reset signal from the host system which is asserted during power up and negated thereafter.
DD0	17	I/O	Drive data bus	16 bit bidirectional data bus between the host and the drive. The lower 8 bits are used for register and ECC byte access. All bits are used for data word transfers.
DD1	15			
DD2	13			
DD3	11			
DD4	9			
DD5	7			
DD6	5			
DD7	3			
DD8	4			
DD9	6			
DD10	8			
DD11	10			
DD12	12			
DD13	14			

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DD14 16
 DD15 18

DIOW- 23 I Drive I/O write Write strobe, the rising edge of which clocks data from the host data bus, DD0 through DD15, into a register or the data port of the drive.

DIOR- 25 I Drive I/O read Read strobe, the falling edge of which enables data from a register or the data port of the drive onto the host data bus, DD0 through DD7 or DD0 through DD15. The rising edge of DIOR- latches data at the host.

DALE 28 I Drive address Address valid indication from the host latch enable system. The host address and chip selects, DAO through DA2, CS1FX-, and CS3FX-, are guaranteed valid on the falling edge of this signal. The address and chip select signals are held valid by the host system after the DALE falling edge, therefore, the drive need not latch these signals with DALE.

TABLE 5.2-1. INTERFACE SIGNAL DESCRIPTION SUMMARY (CONT.)

PIN	PIN				
NAME	NUMBER	I/O	SIGNAL NAME	SIGNAL DESCRIPTION	
INTRQ	31	O	Drive interrupt	Interrupt to the host system, asserted only when the drive CPU has a pending interrupt, the drive is selected, and the host asserts the IEN- bit in the digital output register. When the IEN- bit is negated, or the drive is not selected, this output is in a high impedance state, regardless of the presence or absence of a pending interrupt.	
IOCS16-	32	O	Drive 16 bit I/O	Indication to the host system that the 16 bit data port has been addressed and that the drive is prepared to send or receive a 16 bit data word. This shall be an open collector output.	
DAO	35	I	Drive address	3 bit binary coded address supplied by the DA1 33 bus host when accessing a register or the data	
DA2	36	I	port in the drive.		
PDIAG	34	I/O	PDIAG-	This line will be an input, for the controller designated as the master, and will be used as an output by the slave to indicate that it has successfully passed the diagnostics command. Upon the receipt of a diagnostics command or a reset the slave controller will set this line high. If the command is terminated without error the slave will then set this line low. A "low" will indicate to the master controller (which has this pin programmed as an input) that the slave has passed the diagnostics or completed the reset. The master controller must wait a maximum of 5 seconds from the receipt the diagnostic command or 3 msec after a reset to allow the slave's report of status in the multi-controller mode (DASP- set low). In single controller applications, the master will report status immediately after completion, terminating the command.	
CS1FX-	37	I	Drive chip	Chip select decoded from the host address bus select 0 used to select some of the host accessible registers.	
CS3FX-	38	I	Drive chip	Chip select decoded from the host address bus select 1 used to select some of the host accessible registers.	

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TABLE 5.2-1. INTERFACE SIGNAL DESCRIPTION SUMMARY

PIN NAME	PIN NUMBER	I/O	SIGNAL NAME	SIGNAL DESCRIPTION
DASP-	39	I/O	Drive Active/	Time multiplexed signal which indicates drive Slave Present active or slave present. During a power-up and drive initialization, this line is an output from a slave drive, and an input to a master drive, indicating a slave drive is present. At all times other than during a power up and drive initialization, this line is an output from both master and slave drives which is asserted when the drive is selected and being accessed (BSY is asserted), and may be used to drive an activity LED. This shall be an open collector output.
GND	2	--	Ground Signal	ground returns for the interface lines
	19			
	22			
	24			
	26			
	30			
	40			
RSVD	21	--	Reserved pins.	
	27			
	29			
KEY	20	--	Pin used for keying the interface connector.	

Figure 5.2-1, and 5.2-2 show timing diagrams which define relationships between the interface signals. Timing standards are given for both 16 bit and 8 bit data transfers in Table 5.2-2.

Processor I/O Read, 16 Bit:

DRIVE ADDRESS | ADDRESS VALID
 [1]
 :<-t1->:<-----t2----->:

DIOR-
 : :
 :<-t5-->:<-t6->:

DD0 ...DD15 | DATA VALID
 |

Processor I/O Write, 16 Bit:

DRIVE ADDRESS | ADDRESS VALID
 [1]
 :<-t1->:<-----t2----->:

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DIOW-
: :
: <----t3---->: <-t4->:

DD0 ...DD15 | |DATA VALID
|

[1] Drive Address consists of signals CS1FX, CS3FX, DAO, DA1, DA2 "t" values given in Table 5.2-2.

FIGURE 5.2-1. INTERFACE 16 BIT DATA TRANSFER TO|FROM DRIVE

DALE : :
: <---- t7---->:

IOCS16- :

RESET- : :
: <-t8 ->:

FIGURE 5.2-2. INTERFACE TIMING AFTER A RESET

TABLE 5.2-2. INTERFACE TIMING

SYMBOL	DESCRIPTION	MIN	MAX (16 bit)
t1	Address valid prior to DIOW- or DIOR-	90 nS	---
t2	DIOW- or DIOR- pulse width	165 nS	---
t3	Data valid prior to DIOW- rising edge	140 nS	---
t4	Data hold time after DIOW- rising edge	0 nS	---
t5	Required valid data prior to DIOR- rising edge	95 nS	---
t6	Required data hold time after DIOR- rising edge	5 nS	---
t7	IOCS16- Asserted after rising edge of DALE, 16 bit	---	95 nS
t8	RESET- pulse width	300 nS	---

Note that these are minimum acceptable interface timing requirements.

5.3 PROGRAMMING REQUIREMENTS

5.3.1 General

The drives using this interface shall be programmed by the host computer to perform commands and return status to the host at command completion. When two drives are daisy chained on the interface, commands are written in parallel to both drives, and for all except diagnostic commands, only the selected drive executes the command. With diagnostic commands, both drives execute the command and the slave drive reports its status to the master drive via the PDIAG- signal.

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Drives are selected by the DRV bit in the drive/head register (see section 5.3.2.8), and by a jumper or switch on the drive designating it as either a master or slave. Optionally some drives may provide provision to be jumpered to indicate the drive as a master with no slaves present. When the DRV bit is reset, the master drive is selected, and when the DRV bit is set, the slave drive is selected. When drives are daisy chained, one must be set as the master and one as the slave. When a single drive is attached to the interface it must be set as the master.

Throughout this document, drive selection always refers to the state of the DRV bit, and the position of the master/slave jumper or switch.

5.3.2 I/O Port Descriptions

Input and output to or from the drive is through an I/O Port that routes the input or output data to or from fourteen registers (selected) by a code on the CS1FX-, CS3FX-, DA2, DA1, DA0, DIOR- and DIOW- lines from the Host. Ten of the registers are used for commands to the drive or status, one is the Data Port and three are used for control and alternate status. These are referred to herein as the Command Block Registers and the Control Block Registers. Table 5.3-1 lists these registers and the addresses that select them, together with the functions of addresses that don't select one of the registers.

Logic conventions are 1 = signal asserted; 0 = signal negated; x = does not matter which it is.

TABLE 5.3-1. I/O PORT FUNCTIONS|SELECTION ADDRESSES

ADDRESS		FUNCTIONS				
CS1FX	CS3FX	DA2	DA1	DA0	READ (DIOR- = 1)	WRITE (DIOW- = 1)
1	1	X	X	X	Invalid Address	Invalid Address
0	0	X	X	X	Invalid Address	Invalid Address
0	1	0	X	X	Data Bus High Imped	Not used
0	1	1	0	X	Data Bus High Imped	Not used

Command Block Registers

1	0	0	0	0	Data Port	Data Port
1	0	0	0	1	Error Register	Precomp Cyl. Reg.
1	0	0	1	0	Sector Count Reg.	Sector Count Reg.
1	0	0	1	1	Sector Number Reg.	Sector Number Reg.
1	0	1	0	0	Cylinder Low Reg.	Cylinder Low Reg.
1	0	1	0	1	Cylinder High Reg.	Cylinder High Reg.
1	0	1	1	0	Drive Head Reg.	Drive Head Reg.
1	0	1	1	1	Status Register	Command Register

Control Block Registers

0	1	1	1	0	Alternate Status Reg	Digital Output Reg.
0	1	1	1	1	Drive Address Reg.	Not used

The following paragraphs describe the operations of the registers listed in Table 5.3-1.

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5.3.2.1 Data Port (CS1FX- CS3FX- = 10; DA2 DA1 DA0 = 0; read/write)

The data port is the register through which all data is passed on read and write commands. It is also the port to which the sector table is transferred during format commands. All transfers are high speed 16 bit I/O operations except for ECC bytes transferred during read/write long commands, which are slower 8 bit operations.

5.3.2.2 Error Register (CS1FX- CS3FX- = 10; DA2 DA1 DA0 = 1; read only)

This error register contains status from the last command executed by the drive. The contents of this register are valid only when the error bit (ER) is set in the status register, unless the drive has just powered up or completed execution of its internal diagnostic, in which case the register contains a status code (see section 5.3.2.8). The error bits in the register are defined below:

```

b7      b0
-----
| BBK | UNC | -- | IDNF | -- | ABRT | TKO | AMNF |
-----

```

where BBK indicates a bad block mark was detected in the requested sector's ID field.

UNC indicates an uncorrectable data error has been encountered.

IDNF indicates the requested sector's ID field could not be found.

ABRT indicates the requested command has been aborted due to a drive status error (not ready, write fault, etc.) or because the command code is invalid.

TKO indicates track 0 has not been found during a recalibrate command.

AMNF indicates the data address mark has not been found after finding the correct ID field.

-- not used. These bits are reset to zero.

5.3.2.3 Write Precompensation Cyl. (CS1FX- CS3FX- = 10; DA2 DA1 DA0 = 1; write only)

The starting cylinder for write precompensation is controlled by the contents of this register. The starting physical cylinder is 4 times the value in this register. This register MAY BE ignored by some drives. In this case use of write precompensation is vendor specific.

5.3.2.4 Sector Count (CS1FX- CS3FX- = 10; DA2 DA1 DA0 = 2; read/write)

The sector count defines the number of sectors of data to be read or written. If the value in this register is zero, a count of 256 sectors is specified. This count is decremented as each sector is read so the register contains the number of sectors left to access in the event of an error in a multisector operation. The contents of this register define the number of sectors per track when executing an initialize drive parameters or format command.

5.3.2.5 Sector Number (CS1FX- CS3FX- = 10; DA2 DA1 DA0 = 3; read/write)

This register contains the starting sector number for any disk access. At the completion of each sector, and at the end of the command, this register is updated to reflect the last sector read correctly, or the sector on which an error occurred.

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5.3.2.6 Cylinder Low (CS1FX- CS3FX- = 10; DA2 DA1 DA0 = 4; read/write)

The cylinder low register contains the low order 8 bits of the starting cylinder address for any disk access. At the completion of each sector, and at the end of the command, this register is updated to reflect the current cylinder number.

5.3.2.7 Cylinder High (CS1FX- CS3FX- = 10; DA2 DA1 DA0 = 5; read/write)

The cylinder high register contains the high order bits of the starting cylinder address for any disk access. At the completion of each sector, and at the end of the command, this register is updated to reflect the current cylinder number. The most significant bits of the cylinder address should be loaded into the cylinder high register.

5.3.2.8 Drive/Head (CS1FX- CS3FX- = 10; DA2 DA1 DA0 = 6; read/write)

This register contains the drive and head numbers, as defined below:



DRV is the binary encoded drive selected number. When this bit is negated, the master drive is selected, and when this bit is asserted, the slave drive is selected.

HEAD is the four bit binary encoded head select number.

At the completion of each sector, and at the end of the command, this register is updated to reflect the currently selected head.

5.3.2.9 Status Register (CS1FX- CS3FX- = 10; DA2 DA1 DA0 = 7; read only)

This register contains the drive/controller status. The contents of this register are updated at the completion of each command. If the busy bit is asserted, no other bits are valid. The host reading this register when an interrupt is pending is considered to be the interrupt acknowledge, and any pending interrupt is therefore cleared whenever this register is read. The bits in this register are defined below:



BSY is the busy bit, which is asserted whenever the drive has access to the command block registers, and the host is locked out from accessing the command block. This bit is asserted under the following circumstances:

1. at assertion of the RESET- signal on the interface, or at assertion of the SRST bit in the digital output register.
2. immediately upon host write of the command register with a read, read long, read buffer seek, recal, initialize drive parameters, verify, identify, or diagnostic command.

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3. within 5 microseconds following transfer of 512 bytes of data during execution of a write, format track, or write buffer command, or 512 bytes of data and the appropriate number of ECC bytes during the execution of a write long command.

When BSY is asserted, any host read of a shared register is inhibited and the status register is read instead.

DRDY is the drive ready indication. When there is an error, this bit is not changed until the status register is read by the host, at which time the bit again indicates the current readiness of the drive. This bit should be negated at power up and remain negated until the drive is up to speed and ready to accept a command.

DWF is the drive write fault bit. When there is an error, this bit is not changed until the status register is read by the host, at which time the bit again indicates the current write fault status.

DSC is the drive seek complete bit. This bit is asserted when the disk drive heads are settled over a track. When there is an error, this bit is not changed until the status register is read by the host, at which time the bit again indicates the current seek complete status.

DRQ is the data request bit, which indicates, when asserted, that the drive is ready for transfer of a word or byte of data between the host and the data port.

CORR is the corrected data bit, which is asserted when a correctable data error has been encountered and the data has been corrected. This condition does not terminate a multisector read operation.

IDX is the index bit which is asserted once per disk revolution.

ERR is the error bit, which indicates when asserted that the previous command ended in some type of error. The other bits in the status register, and the bits in the error register have additional information as to the cause of the error.

5.3.2.10 Command Register (CS1FX- CS3FX- = 10; DA2 DA1 DA0 = 7, write only)

The eight bit code written to this register transfers to the drive the command that the host is requesting. Command execution begins immediately after this register is written. A list of executable commands with the command codes and necessary parameters for each command follows.

COMMAND CODE	PARAMETERS USED
COMMAND NAME	b7 b0 PC SC SN CY DH

recalibrate	0001 xxxx n n n n D
read sector(s)	0010 00LR n y y y y
write sector(s)	0011 00LR n y y y y
read verify sector(s)	0100 000R n y y y y
format track	0101 0000 n y n y y
seek	0111 xxxx n n n y y
execute drive diagnostic	1001 0000 n n n n D
initialize drive	1001 0001 n y n n y
parameters	

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```

read sector buffer | 1 1 1 0 0 1 0 0 | n n n n D |
write sector buffer   | 1 1 1 0 1 0 0 0 | n n n n D |
identify drive       | 1 1 1 0 1 1 0 0 | n n n n D |
set buffer mode      | 1 1 1 0 1 1 1 1 | n n n n n |
read multiple        | 1 1 0 0 0 1 0 0 | n y y y y |
write multiple       | 1 1 0 0 0 1 0 1 | n y y y y |
set multiple mode    | 1 1 0 0 0 1 1 0 | n y n n D |
|-----|

```

L is the long bit, if 1, read/write long commands are executed, if 0, normal read/write commands are performed.

R is the retry bit, if 0, retries are enabled, if 1, retries are disabled.

PC is the write precomp register.

SC is the sector count register.

SN is the sector number register.

CY is the cylinder registers.

DH is the drive/head register

y means the register contains a valid parameter for this command. For the drive|head register, y means that both the drive and head parameters are used.

n means the register does not contain a valid parameter for this command.

D means only the drive parameter is valid and not the head parameter.

x is a don't care.

5.3.2.11 Alternate Status (CS1FX- CS3FX- = 01; DA2 DA1 DA0 = 6; read only)

This register contains the same information as the status register in the command block. The only difference being that reading this register does not imply interrupt acknowledge or reset a pending interrupt.

b7 b0

```

| BSY | DRDY | DWF | DSC | DRQ | CORR | IDX | ERR |
|-----|

```

See section 5.3.2.9 for definitions of the bits in this register.

5.3.2.12 Digital Output (CS1FX- CS3FX- = 01; DA2 DA1 DA0 = 6; write only)

This register contains two control bits as follows:

b7 b0

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| -- | -- | -- | -- | -- | SRST | IEN- | -- |

IEN- is the enable bit for the disk drive interrupt to the host. When this bit is asserted, and the drive is selected, the host interrupt, INTRQ, is enabled, through a tri-state buffer, to the host. When this bit is negated, or the drive is not selected the INTRQ pin is in a high impedance state, regardless of the presence or absence of a pending interrupt.

SRST is the host software reset bit. The drive is held reset when this bit is asserted, and enabled when this bit is negated. If two drives are daisy chained on the interface, this bit resets and enables both drives simultaneously.

-- these bits are not used.

5.3.2.13 Drive Address (CS1FX- CS3FX- = 01; DA2 DA1 DA0 = 7; read only)

This port loops back the drive select and head select addresses of the currently selected drive. The bits in this port are as follows:

b7 b0

 | RSVD | WTG- | HS3- | HS2- | HS1- | HS0- | DS1- | DS0- |

RSVD is reserved and undriven by the drive. When the host reads the drive address register, this bit must be in a high impedance state.

WTG- is the write gate bit, which is asserted when writing to the disk drive is in progress.

HS3- through HS0- are the one's complement of the binary coded address of the currently selected head. For example, if HS3- through HS0- are 1 1 0 0, respectively, head 3 is selected. HS3- is the most significant bit.

DS1- is the drive select bit for drive 1, and should be asserted when drive 1 is selected and active.

DS0- is the drive select bit for drive 0, and should be asserted when drive 0 is selected and active.

CAUTION

Use care interpreting these bits, as they do not always represent the expected status of drive operations at the instant the status was put into this register. This is because of the use of caching, translate mode and the master/slave concept with each drive having its own embedded controller.

5.3.3 Reset Response

When the drive is reset, either by the host reset interface pin, RESET-, or by the host software reset bit, SRST, in the digital output register, the drive asserts BSY immediately. Once the reset has been removed and the drive has been reenabled, with BSY still asserted, the drive performs any necessary hardware initialization, clears any previously programmed drive parameters and reverts to the default condition, loads the command block registers with their initial values, and then negates BSY.

No interrupt is generated when initialization is complete, and no self test is performed. The initial values (hex) for the command block registers are as follows:

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Error register = 01
Sector Count = 01
Sector Number = 01
Cylinder Low = 00
Cylinder High = 00
Drive|Head register = 00

5.3.4 Command Information

Commands are issued to the drive by loading the pertinent registers in the command block with the needed parameters, asserting the interrupt enable bit, IEN- in the digital output register, and then writing the command code to the command register. Execution begins as soon as the command register is written.

5.3.4.1 Error Reporting

The errors that are valid (although valid, it is not a requirement that all valid conditions be implimented) for each command are defined in the matrix below:

	BBK	UNC	IDNF	ABRT	TK0	AMNF	DRDY	DWF	DSC	CORR	ERR
RECALIBRATE	V	V	V	V	V	V					
READ SECT	V	V	V	V	V	V	V	V	V	V	V
READ LONG	V	V	V	V	V	V					
WRITE SECT	V	V	V	V	V	V					
WRITE LONG	V	V	V	V	V	V					
READ VERIFY	V	V	V	V	V	V	V	V	V	V	V
FORMAT TRK	V	V	V	V	V	V					
SEEK	V	V	V	V	V	V					
DRIVE DIAG	V										
INIT DRIVE PARMS											
READ BUFFER											
WRITE BUFFER											
IDENTIFY DRIVE	V	V	V	V	V	V					
INVALID CMD CODE	V										
SET BUFFER MODE	V										
READ MULTIPLE	V	V	V	V	V	V	V	V	V	V	V
WRITE MULTIPLE	V	V	V	V	V	V	V	V			
SET MULTIPLE MODE	V										

BBK is bad block detected
UNC is uncorrectable data error
IDNF is requested ID not found
ABRT is aborted command error
TK0 is track 0 not found error
AMNF is data address mark not found error
DRDY is disk drive not ready detected
DWF is disk drive write fault detected
DSC is disk drive seek complete not detected
CORR is corrected data error
ERR is the error bit in the status register
V means error type is valid for this command

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5.3.5 Translate Mode

The translate mode is optional and device specific. The drive firmware translates logical sector requests from the host into corresponding physical sector requests. In the nontranslate mode, the drive is accessed based on its actual physical parameters.

5.3.6 Command Descriptions

The drive shall implement the following mandatory commands:

- Recalibrate
- Read Sector(s)
- Write Sector(s)
- Read Verify Sector(s)
- Format desired track
- Seek
- Execute Drive Diagnostic
- Initialize Drive Parameters

The drive may implement the following optional commands:

- Read Buffer
- Write Buffer
- Identify Drive
- Set Buffer Mode
- Read Multiple
- Write Multiple
- Set Multiple Mode

5.3.6.1 Recalibrate (M)

This command moves the read|write heads from anywhere on the disk to cylinder 0. Upon receipt of the command, the drive asserts BSY and issues a seek to cylinder zero. The drive then waits for the seek to complete before updating status, negating BSY and generating an interrupt. If the drive cannot reach cylinder 0, the error bit is asserted in the status register, and the track 0 bit asserted in the error register.

5.3.6.2 Read Sector(s). (M)

This command reads from 1 to 256 sectors as specified in the command block (sector count equal to 0 requests 256 sectors), beginning at the specified sector. As soon as the command register is written, the drive asserts the BSY bit and begins execution of the command. If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, the drive searches for the appropriate ID field. If retries are disabled and two index pulses have occurred without error free reading of the requested ID, an ID not found error is posted in the error register. If retries are enabled, up to a vendor specific number of attempts may be made to read the requested ID before reporting an error. If the ID is read correctly, the data address mark must be recognized within a specified number of bytes, or the data address mark not found error is reported. Once the data address mark is found, the data field is read into the sector buffer, error bits are asserted if an error was encountered, the DRQ bit is asserted, and an interrupt is generated. The DRQ bit is always asserted regardless of the presence or absence of an error condition at the end of the sector. Upon command completion, the command block registers contain the cylinder, head, and sector number of the last sector read.

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Multiple sector reads assert DRQ and generate an interrupt when the sector buffer is filled at the completion of each sector, and the drive is ready for the data to be read by the host. DRQ is negated and BSY is asserted immediately when the host empties the sector buffer. If an error occurs during a multiple sector read, the read terminates at the sector where the error occurs. The command block registers contains the cylinder, head, and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector. If the error was either a correctable data error or an uncorrectable data error, the flawed data is loaded into the sector buffer.

A read long is executed by setting the long bit in the command code. The read long command returns the data and the ECC bytes contained in the data field of the desired sector. During a read long, the drive does not check the ECC bytes to determine if there has been any type of data error. Only single sector read long operations are supported.

5.3.6.3 Write Sector(s) (M)

This command writes from 1 to 256 sectors as specified in the command block (sector count equal to 0 requests 256 sectors), beginning at the specified sector. As soon as the command register is written, the drive asserts the DRQ bit and waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first buffer fill operation. Once the buffer is full, the drive negates DRQ, asserts BSY and begins command execution. If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, the drive searches for the appropriate ID field. If retries are disabled and two index pulses have occurred without error free reading of the requested ID, an ID not found error is posted in the error register. If retries are enabled, up to a vendor specific number of attempts may be made to read the requested ID before reporting an error. If the ID is read correctly, the data loaded in the buffer is written to the data field of the sector, followed by the ECC bytes. Upon command completion, the command block registers contain the cylinder head, and sector number of the last sector read.

Multiple sector writes assert DRQ and generate an interrupt each time the buffer is ready to be filled. DRQ is negated and BSY is asserted immediately when the host fills the sector buffer. If an error occurs during a multiple sector write, writing terminates at the sector where the error occurs. The command block registers contain the cylinder, head, and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

A write long is executed by setting the long bit in the command code. The write long command writes the data and the ECC bytes directly from the sector buffer; the drive does not generate the ECC bytes itself. Only single sector write long operations are supported.

5.3.6.4 Read Verify Sector(s) (M)

This command is identical to the read sectors command, except that DRQ is never asserted, no data is transferred to the host and the long bit is not valid. The drive asserts BSY as soon as the command register is written and negates BSY and generates an interrupt when the requested sectors have been verified. Upon command completion, the command block registers contain the cylinder, head, and sector number of the last sector verified.

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If an error occurs during a multiple sector verify, the read terminates at the sector where the error occurs. The command block registers contain the cylinder, head, and sector number of the sector where the error occurred.

5.3.6.5 Format Track (M)

If a Format Track command is issued to the drive, it will react differently depending on whether the logical or physical mode had been previously indicated by the set parameters command:

This command formats the track specified in the command block, with the number of sectors specified in the sector count register. As soon as the command register is written, the drive sets the DRQ bit and waits for the host to fill the sector buffer with the interleave table. When the buffer is full, the drive negates DRQ, asserts BSY and begins command execution. If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, the ID'S are written using the interleave table from the sector buffer and the data fields are written with all zeroes. Formatting begins as soon as the index pulse is detected, by writing the first physical sector with the logical sector number in the first entry of the interleave table. Subsequent physical sectors are formatted in turn from the table. Media defects are marked bad on a sector level, allowing the remainder of the track to be used. When the specified number of sectors have been formatted, the drive fills the remainder of the track to index with gap bytes. At the completion of the track, the drive negates BSY and generates an interrupt.

The interleave table is made up of two bytes per sector on the track. The first byte is 00 if the sector is to be formatted normally, or 80h if the sector is to be formatted bad. The second byte is the logical sector number of the sector. After writing the interleave table, additional bytes should be loaded into the buffer until it is full (512 bytes). The contents of a typical interleave table are shown below, for a 27 sector track with an interleave of 1 and sector 3 marked bad.

```
00 01 00 02 80 03 00 04 00 05 00 06 00 07 00 08
00 09 00 0A 00 0B 00 0C 00 0D 00 0E 00 0F 00 10
00 11 00 12 00 13 00 14 00 15 00 16 00 17 00 18
00 19 00 1A 00 1B dd dd dd dd dd dd dd dd dd dd
dd dd dd dd dd dd dd dd dd dd dd dd dd dd dd
dd dd dd dd dd dd dd dd dd dd dd dd dd dd dd
.
.
.
.
dd dd dd dd dd dd dd dd dd dd dd dd dd dd dd
```

dd is a don't care byte used to make up a total of 512 bytes

5.3.6.6 Seek (M)

This command initiates a seek to the track and selects the head specified in the command block. The drive need not be formatted for a seek to execute properly. When the command is issued, the drive asserts BSY in the status register, initiates the seek, negates BSY, and generates an interrupt. The seek is not completed before the drive returns the interrupt. If a new command is issued to a drive while a seek is being executed, the drive delays with BSY asserted for the seek to complete before executing the new command.

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5.3.6.7 Execute Drive Diagnostic (M)

This command performs the internal diagnostic tests implemented by the drive. The diagnostic tests shall be executed only upon receipt of this command. They shall not be executed automatically at power up or after a reset.

The drive asserts BSY immediately upon receipt of the command. If the drive is a master, it does not drive the disk active/slave present signal, DASP-, during diagnostics and if the drive is a slave, it drives DASP- to the asserted state. The drive then performs the diagnostic tests and saves the results. If the drive is a master and a slave is connected, it waits up to 5 seconds for the slave to complete its diagnostics and then reports the diagnostic results for a connected slave drive. If the drive is a master and no slave is present, it reports only its own diagnostic results. Once the slave reporting requirement, if any, is met, the drive negates BSY, and generates an interrupt. The value in the error register should be viewed as a unique 8 bit code and not as the single bit flags defined in section 5.3.2.2. Table 5.3-3 below details the codes and the corresponding explanation:

TABLE 5.3-3. ERROR CODES

Error Code	Description
01	no error detected
02	formatter device error
03	sector buffer error
04	ECC circuitry error
05	controller microprocessor error
8x	slave drive failed (see note)

Note: If the slave drive fails diagnostics, the master drive "ORs" gates 80 hex with its own status and loads that code into the error register. If the slave drive passes diagnostics or there is no slave drive connected, the master drive "ORs" 00 with its own status and loads that code into the error register.

5.3.6.8 Initialize Drive Parameters (M)

This command enables the host to control certain drive parameters. Some parameters are standard while others are vendor specific. Table ?? enumerates the register values for this function.

(TABLE TBD)

5.3.6.9 Read Buffer (O)

The read buffer command enables the host to read the current contents of the drive's sector buffer. When this command is issued, the drive asserts BSY, sets up the sector buffer for a read operation asserts DRQ, negates BSY, and generates an interrupt. The host then reads up to 512 bytes of data from the buffer.

5.3.6.10 Write Buffer (O)

The write buffer command enables the host to overwrite the contents of the drive's sector buffer with any data pattern desired. When this command is issued, the drive asserts BSY, sets up the sector buffer for a write operation, asserts DRQ, negates BSY, and generates an interrupt. The host then writes up to 512 bytes of data to the buffer.

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5.3.6.11 Identify Drive (O)

The identify command enables the host to receive parameter information from the drive. When the command is issued, the drive asserts BSY, stores the required parameter information in the sector buffer, asserts the DRQ bit, and generates an interrupt. The host then reads the information out of the sector buffer. The parameter words in the buffer have the following arrangement and meanings, all reserved bits or words should be zeroes.

Word 0 General configuration
Word 1 Number of fixed cylinders
Word 2 Reserved
Word 3 Number of heads
Word 4 Number of unformatted bytes per physical track
Word 5 Number of unformatted bytes per sector
Word 6 Number of physical sectors per track
Word 7
: Reserved
9
Word 10
: Serial number (20 ASCII characters, Oh - not specified).
Word 19
Word 20 Controller type
0000 not specified
0001 single ported single sector buffer
0002 dual ported multiple sector buffer
0003 dual ported multiple sector buffer with look-ahead read
0004
: reserved
FFFF
Word 21 Controller buffer size in 512 byte increments (Oh - not specified).
Word 22 Number of ECC bytes passed on read|write long commands (Oh - not specified).
Word 23
: Controller firmware revision (8 ASCII characters, Oh = not specified).
Word 26
Word 27
: Model number (40 ASCII characters, Oh = not specified).
Word 46
Word 47 Number of sectors that can be transferred per interrupt on read and write multiple commands (0 = read|write multiple commands not implemented).
Word 48 Doubleword I/O capability, 0 = cannot perform doubleword I/O, 1 = can perform doubleword I/O.
Word 49
: Reserved
Word 255

5.3.6.11 continued

The bits in the general configuration word have the following definitions:

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Bit 0	Reserved
Bit 1	1=hard sectored
Bit 2	1=soft sectored
Bit 3	1=not MFM encoded
Bit 4	1=head switch time greater than 15 us
Bit 5	1=spindle motor control option implemented
Bit 6	1=fixed drive
Bit 7	1=removable cartridge drive
Bit 8	1=transfer rate less than or equal to 5Mb s
Bit 9	1=transfer rate greater than 5Mb s bus less than or equal to 10Mb s
Bit 10	1=transfer rate greater than 10Mb s
Bit 11	1=rotational speed tolerance is greater than .5%
Bit 12	0
Bit 13	0
Bit 14	1
Bit 15	0

5.3.6.12 Set Buffer Mode Command (O)

This command enables or disables the read look-ahead feature. Prior to command issuance, the write precompensation register should be loaded with either AAh, to enable, or 55h, to disable read look-ahead operation. Upon receipt of the command, the controller asserts and checks at the write precompensation register contents. If the register contents are either 55h or AAh, the appropriate mode is selected. Any other value in the register results in an aborted command. At command completion, the controller negates BSY and generates an interrupt. At power up, or after a software or hardware reset, the default mode is read look-ahead enabled.

5.3.6.13 Read Multiple Command (O)

The read multiple command performs similarly to the read sectors command except that data transfers are multiple sector blocks and the long bit is not valid. Command execution is identical to the read sectors operation but with several sectors transferred to the host as a block without intervening interrupts and requiring only DRQ qualification of the transfer at the start of the block, not on each sector. The block count, which is the number of sectors to be transferred as a block, is programmed by the set multiple mode command, which must be executed prior to the read multiple command. When the read multiple command is issued, the sector count register contains the number of sectors (not the number of blocks or the block count) requested. If this sector count is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer will be for N sectors, where

$$N = (\text{sector count}) \text{ modulo } (\text{block count}).$$

If the read multiple command is attempted before the set multiple mode command has been executed or when read multiple commands are disabled, the read multiple operation will be rejected with an aborted command error.

Disk errors encountered during read multiple commands are reported at the beginning of the block or partial block transfer, but DRQ is still asserted and the transfer will take place as it normally would, including transfer of corrupted data, if any. Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the

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block which contained the error. Interrupts are generated when DRQ is asserted at the beginning of each block or partial block.

5.3.6.14 Write Multiple Command (O)

The write multiple command performs similarly to the write sectors command except that the controller asserts BSY immediately upon receipt of the command, data transfers are multiple sector blocks, and the long bit is not valid. Command execution is identical to the write sectors operation but with several sectors transferred to the host as a block without intervening interrupts and only requiring DRQ qualification of the transfer at the start of the block, not on each sector. The block count, which is the number of sectors to be transferred, is programmed by the set multiple mode command, which must be executed prior to the write multiple command. When the write multiple command is issued, the sector count register contains the number of sectors (not the number of blocks or the block count) requested. If this sector count is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for N sectors, where

$$N = (\text{sector count}) \text{ modulo } (\text{block count}).$$

If the write multiple command is attempted before the set multiple mode command has been executed or when write multiple commands are disabled, the write multiple operation shall be rejected with an aborted command error.

All disk errors encountered during write multiple commands are reported after the attempted disk write of the block or partial block transferred. The write operation ends with the sector in error, even if it was in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is asserted at the beginning of each block or partial block.

5.3.6.15 Set Multiple Mode Command (O)

This command enables the controller to perform read and write multiple operations and establishes the block count for these commands. Prior to command issuance, the sector count register should be loaded with the number of sectors per block. Controllers shall support block sizes of 2, 4, 8, and 16 sectors, if their buffer size is at least 8k bytes, and may also support other block sizes. Upon receipt of the command, the controller asserts BSY and checks the sector count register contents. If the register contents are a valid and the block count is supported, the value is loaded for all subsequent read and write multiple commands and execution of those commands is enabled. Any unsupported block count in the register results in an aborted command error and read and write multiple commands being disabled. If the sector count register contains 0 when the command is issued, read and write multiple commands are disabled. Once the appropriate action has been taken, the controller negates BSY and generates an interrupt. At power up, or after a hardware or software reset, the default mode is read and write multiple disabled.