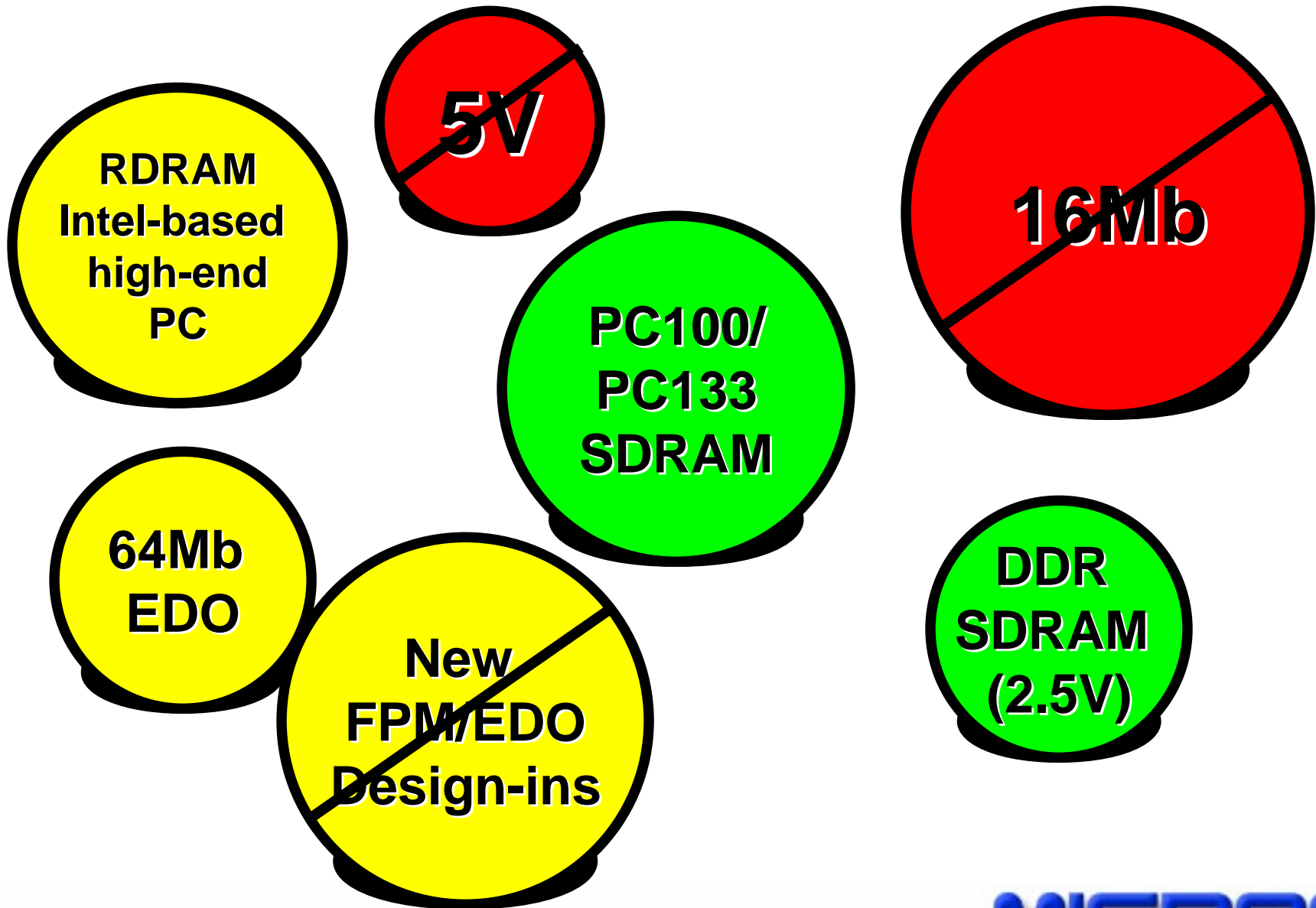


DRAM Design Guide For 5+ Years Compliance

DRAM Trends



DRAM Design Guidelines

Options	Package	Width	Data Rate	Voltage	I/O	16Mb	64Mb	128Mb	256Mb	512Mb	Clock (MHz)
1	54 TSOP	x4	SDR	3.3V	LVTTL	na	16 Meg x 4	32 Meg x 4	64 Meg x 4	128 Meg x 4	PC100/133
2	54 TSOP	x8	SDR	3.3V	LVTTL	na	8 Meg x 8	16 Meg x 8	32 Meg x 8	64 Meg x 8	PC100/133
3	54 TSOP	x16	SDR	3.3V	LVTTL	na	4 Meg x 16	8 Meg x 16	16 Meg x 16	32 Meg x 16	PC100/133
4	50 TSOP	x16	SDR	3.3V	LVTTL	1 Meg x 16	na	na	na	na	143/166/200
5	86 TSOP	x32	SDR	3.3V	LVTTL	na	2 Meg x 32	4 Meg x 32	8 Meg x 32	TBD	143/166/200
6	66 TSOP	x4	DDR	2.5V	SSTL_2	na	16 Meg x 4	32 Meg x 4	64 Meg x 4	128 Meg x 4	PC200/266
7	66 TSOP	x8	DDR	2.5V	SSTL_2	na	8 Meg x 8	16 Meg x 8	32 Meg x 8	64 Meg x 8	PC200/266
8	66 TSOP	x16	DDR	2.5V	SSTL_2	na	4 Meg x 16	8 Meg x 16	16 Meg x 16	32 Meg x 16	PC200/266
9	100 TQFP	x32	DDR-SG	2.5V	SSTL_2	512K x 32	na	na	na	na	150/166
	100 TQFP	x32	DDR	2.5V	SSTL_2	na	2 Meg x 32	4 Meg x 32	8 Meg x 32	TBD	166/183

Minimum Granularity (MB) vs. Bus Width

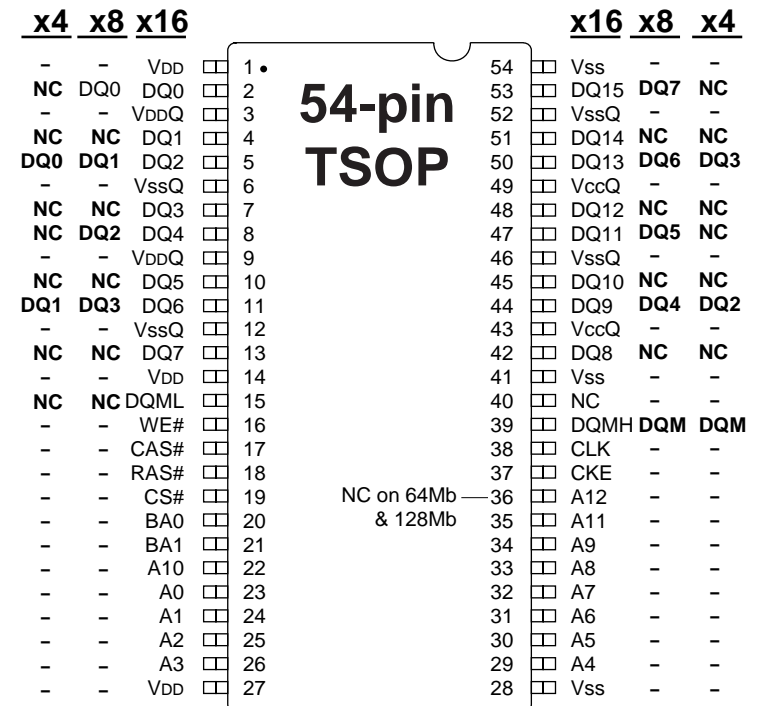
Package	Width	16-Bit Bus Width				32-Bit Bus Width				64-Bit Bus Width			
		16Mb	64Mb	128Mb	256Mb	16Mb	64Mb	128Mb	256Mb	16Mb	64Mb	128Mb	256Mb
54 TSOP	x4	--	32	64	128	--	64	128	256	--	128	256	512
54 TSOP	x8	--	16	32	64	--	32	64	128	--	64	128	256
54 TSOP	x16	--	8	16	32	--	16	62	64	--	32	64	128
50 TSOP	x16	2	--	--	--	4	--	--	--	8	--	--	--
86 TSOP	x32	--	8	16	32	--	8	16	32	--	16	32	64
66 TSOP	x4	--	32	64	128	--	64	128	256	--	128	256	512
66 TSOP	x8	--	16	32	64	--	32	64	128	--	64	128	256
66 TSOP	x16	--	8	16	32	--	16	32	64	--	32	64	128
100 PQFP	x32	2	--	--	--	2	--	--	--	4	--	--	--
100 PQFP	x32	--	8	16	32	--	8	16	32	--	16	32	64

DRAM Design Guidelines

Options	Package	Width	Data Rate	Voltage	I/O	16Mb	64Mb	128Mb	256Mb	512Mb	Clock (MHz)
1	54 TSOP	x4	SDR	3.3V	LVTTTL	na	16 Meg x 4	32 Meg x 4	64 Meg x 4	128 Meg x 4	PC100/133
2	54 TSOP	x8	SDR	3.3V	LVTTTL	na	8 Meg x 8	16 Meg x 8	32 Meg x 8	64 Meg x 8	PC100/133
3	54 TSOP	x16	SDR	3.3V	LVTTTL	na	4 Meg x 16	8 Meg x 16	16 Meg x 16	32 Meg x 16	PC100/133

□ 54-pin TSOP

- SDR (Single Data Rate)
- Medium to large memory arrays
- PC main memory chief user
- $t_{WR} = 2$ clocks
- 512Mb uses same package/ pinout, per se
- 512Mb refresh - 64ms period
- $t_{RFC} = 1.6 \times t_{RC}$



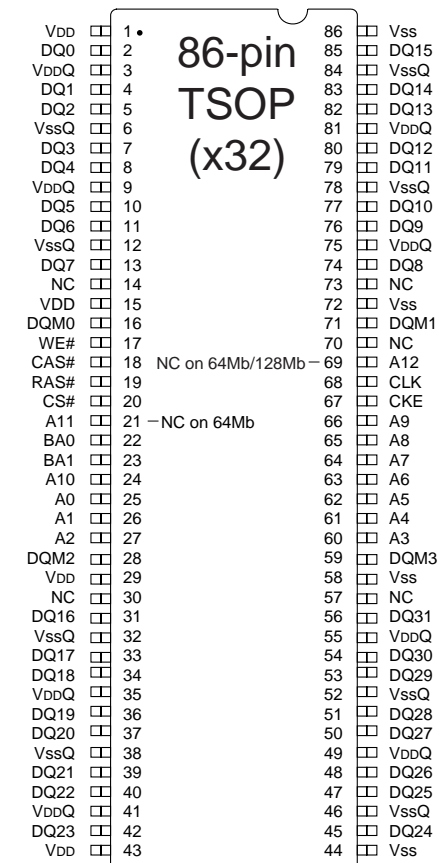
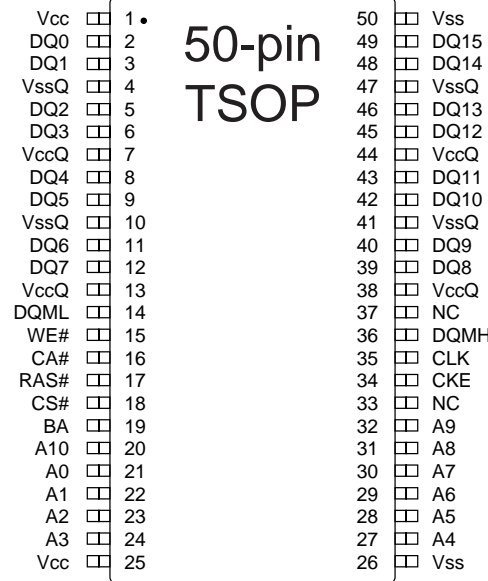
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DRAM Design Guidelines

Options	Package	Width	Data Rate	Voltage	I/O	16Mb	64Mb	128Mb	256Mb	512Mb	Clock (MHz)
4	50 TSOP	x16	SDR	3.3V	LVTTTL	1 Meg x 16	na	na	na	na	143/166/200
5	86 TSOP	x32	SDR	3.3V	LVTTTL	na	2 Meg x 32	4 Meg x 32	8 Meg x 32	TBD	143/166/200

❑ 50 and/or 86 TSOP

- SDR (Single Data Rate)
- Minimum memory arrays
- PC graphics chief user
- $t_{WR} = 2$ clocks



SDRAM Addressing

SDRAM	Addressing	x4	x8	x16	x32
64Mb ^a (4 banks)	Row	A0-A11	A0-A11	A0-A11	A0-A10
	Column	A0-A9	A0-A8	A0-A7	A0-A7
128Mb ^a (4 banks)	Row	A0-A11	A0-A11	A0-A11	A0 -A11 ^d
	Column	A0-A9, A11	A0-A9	A0-A8	A0-A7
256Mb ^a (4 banks)	Row	A0-A12 ^{b,c}	A0-A12 ^{b,c}	A0-A12 ^{b,c}	A0-A12 ^e
	Column	A0-A9, A11	A0-A9	A0-A8	A0-A7
512Mb ^a (4 banks)	Row	A0-A12 ^{b,c}	A0-A12 ^{b,c}	A0-A12 ^{b,c}	TBD
	Column	A0-A9, A11, A12 ^{b,c}	A0-A9, A11	A0-A9	TBD

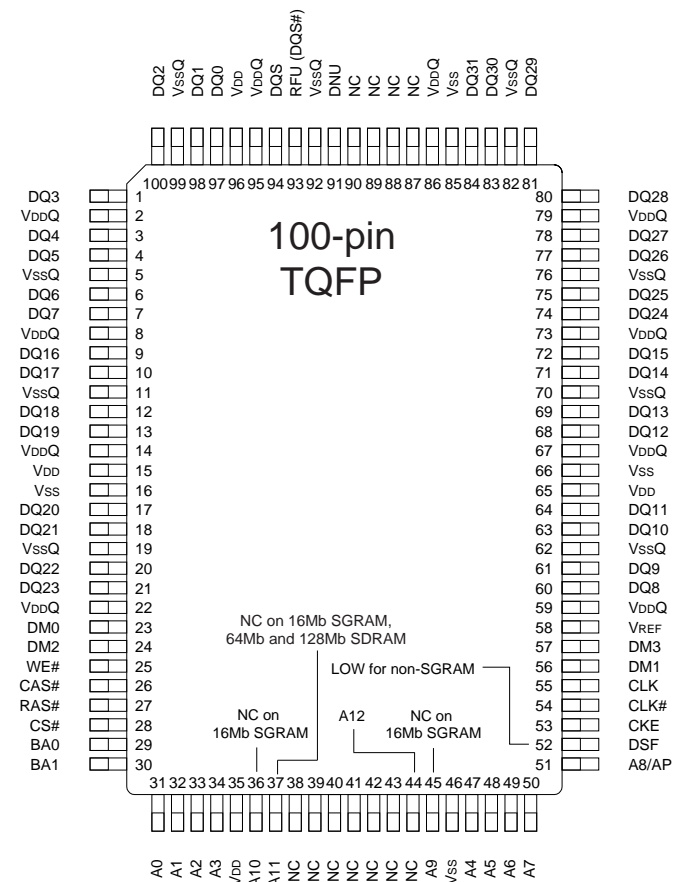
- a. **54-pin TSOP** (x4, x8, x16) and **86-pin TSOP** (x32)
- b. Refresh goes from 15.625µs per row to 7.8µs per row
- c. Pin 36 goes from NC to A12
- d. Pin 21 goes from NC to A11
- e. Pin 69 goes from NC to A12

DRAM Design Guidelines

Options	Package	Width	Data Rate	Voltage	I/O	16Mb	64Mb	128Mb	256Mb	512Mb	Clock (MHz)
9	100 TQFP	x32	DDR-SG	2.5V	SSTL_2	512K x 32	na	na	na	na	150/166
	100 TQFP	x32	DDR	2.5V	SSTL_2	na	2 Meg x 32	4 Meg x 32	8 Meg x 32	TBD	166/183

□ 100-pin TQFP

- **DDR (Double Data Rate) provides data at two times the clock rate**
- **Minimum memory arrays**
- **High-end graphics and routers will be chief users**
- **$t^*_{WR} = 2.5$ clocks**



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DDR SDRAM Addressing

SDRAM	Addressing	x4	x8	x16	x32
16Mb ^a (2 banks)	Row	—	—	—	A0-A8
	Column	—	—	—	A0-A7
64Mb ^b (4 banks)	Row	A0-A11	A0-A11	A0-A11	A0-A10 ^d
	Column	A0-A9	A0-A8	A0-A7	A0-A7
128Mb ^b (4 banks)	Row	A0-A11	A0-A11	A0-A11	A0-A11 ^f
	Column	A0-A9, A11	A0-A9	A0-A8	A0-A7
256Mb ^b (4 banks)	Row	A0-A12 ^{c,e}	A0-A12 ^{c,e}	A0-A12 ^{c,e}	A0-A12 ^g
	Column	A0-A9, A11	A0-A9	A0-A8	A0-A7
512Mb ^b (4 banks)	Row	A0-A12 ^{c,e}	A0-A12 ^{c,e}	A0-A12 ^{c,e}	A0-A12 ^g
	Column	A0-A9, A11, A12	A0-A9, A11	A0-A9	A0-A7, A9

- a. **100-pin TQFP** (x32), SGRAM only
- b. **66-pin TSOP** (x4, x8, x16) and **100-pin TQFP** (x32; SDRAM only with pin 52 = low)
- c. Pin 42 goes from NC to A12
- d. Pin 45 goes from NC to A9; pin 36 goes from NC to A10
- e. Refresh goes from 15.625µs per row to 7.8µs per row
- f. Addressing not finalized, pin 37 goes from NC to A11
- g. Addressing not finalized, pin 44 goes from NC to A12



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