

PC100

White Paper

Synchronous DRAM and

Unbuffered Synchronous

DIMMs



Index

		Page
1	Introduction	2
2	System Clock Rates, CAS Latency - Impact and Relevance	3
3	PC100 Standard, What is it exactly?	5
4	PC100 Features and Benefits, Design Issues	6
5	BIOS Options, Standards within standards – PC100 options, SPD Programming	8
6	SPD Permanent Write - DIMM Options	10
7	DIMM Manufacturing	11
8	Disclaimer	12

Introduction

The PC100 specification has been introduced by Intel to define the standards for a new generation of DRAMs and DRAM modules, which can support a system motherboard clock rate of 100MHz. It is worth noting that Intel has introduced and promoted this standard to ensure a plentiful supply of high quality DRAM modules for its new 100MHz chipset. However a 100MHz system clock rate will also be supported by chip sets from Acer Laboratories Inc – the *Aladdin Pro II*, SIS (Silicon Integrated Systems Corporation) with the *Archer Chip Set* and VIA Technologies new *Apollo Pro*. These too will need PC100 compliant DRAM DIMMs.

This paper introduces the changes being brought about by these new chipsets and the impact that they are having on memory modules.

Significance

The introduction of PC100 is significant because the standard is difficult and expensive to achieve. Customers currently enjoy an almost infinite source of DRAM modules today but this is likely to be drastically reduced by the introduction of 100MHz performance requirements, at least in the short to medium term.



System Clock Rates – Impact and Relevance

The clock rate, measured in MHz (megahertz) is the most commonly used definition for a PCs performance. End users have become used to asking what clock rate a processor is and the Intel clock rate has become a standard for clone CPU manufacturers via the 'P' rating system. However the processor over all clock rate is defined by the speed at which the components can run on the motherboard. This is known as the system clock rate.

The table below illustrates the changes that have taken place in system clock rates to allow the introduction of faster and faster processors.

System Bus Clock Rate	Multiplier	CPU	CPU Clock Rate
33MHz	X 1	486DX-33	33MHz
33MHz	X 2	486DX2-66	66MHz
33MHz	X 3	486DX4-100	100MHz
60MHz	X 1.5	Pentium P75	75MHz
66MHz	X 1.5	Pentium P100	100MHz
60MHz	X 2	Pentium P120	120MHz
66MHz	X 2	Pentium P133	133MHz
60MHz	X 2.5	Pentium P150	150MHz
66MHz	X2.5	Pentium P166	166MHz
66MHz	X 3	Pentium P200	200MHz
66MHz	X 3.5	Pentium P233	233MHz
66MHz	X 3.5	Pentium II P233	233MHz
66MHz	X 4	Pentium II P266	266MHz
66MHz	X 5	Pentium II P300	300MHz
66MHz	X 6	Pentium II P333	333MHz
100MHz	X 3.5	To be announced	350MHz
100MHz	X 4	To be announced	400MHz
100MHz	X 4.5	To be announced	450MHz

It was becoming impossible to keep increasing CPU MHz without bringing up the rest of the system performance. The table above makes this obvious. The introduction of the new 100MHz chipset from Intel and the drive to 100MHz system performance was thus inevitable.

The increase in multiplication for the system x CPU clock rates has made a major impact on the memory subsystem.

The Processor has to be 'fed' data from system RAM. This has to happen for each bus cycle. Cache RAM was introduced to sit between the CPU and system RAM to make sure that this takes place. At 66MHz system clock the memory bus cycle is 15nS and 60nS EDO DRAM could not keep up. Pipeline burst cache was introduced to help fill the gap.

But there is a problem with this set up.

The Processor and cache try to work on the basis that the faster cache RAM stores the data that the processor is going to need. Unfortunately 3-4% of the time this does not happen and the CPU has to search the slower DRAM to find the data, the processor then has to effectively stop whilst it waits for the data to turn up (known as wait states) and this significantly slows up the computer.



Synchronous DRAM was thus introduced which allows great 'chunks' (whole words) of data to be sent directly to the processor at speeds similar to that of pipeline burst cache BUT *direct from the main system RAM*. Here the issue is not the standard access time of the DRAM but something called the **CAS Latency**. Indicated by the letters 'CL'.

CAS Latency Explained

The DRAM industry has become used to measuring DRAM performance by the standard access time in nano-seconds (nS), for example the Vanguard EDO 4MX32 SIMM is described as being available in either 70nS or 60nS variants.

ALL PC100 DIMMs however will be marked as 10nS, 100MHz. But they won't all perform the same. When the CPU asks the system RAM for data it does so by issuing a read command (on a rising clock edge). The delay between the *issuing* of the request and the *actioning* of the request is the CAS latency. CL is measured in clock cycles. The less needed the faster the DIMM. Usually the CL is determined by the speed of the motherboard. Early DIMMs perform as follows;

Standard SYNC DIMMs

CL1 @ 33MHz, CL2 @ 66MHz, CL3 @ 100MHz.

However the better performing DIMMs can produce a CL2 @ 100MHz.

Why is all the above relevant?

The Pentium II cartridge includes the processor and cache in a module. Therefore the SDRAM is interfaced directly from the module, now at over a 100MHz. Signals are propagated at rates that make them highly sensitive. Subtle design issues have become critical.

For example trace length – the measurement of the 'wires' within the Printed Circuit Board (PCB) – for the SDRAM DIMM module has become crucial. With standard EDO DIMM's it was possible to manufacture standard PCB's with the most lazy designs for less than \$1.50. It was this that led to the explosion of Third Party SIMM Manufacturers (TPSMs) in the USA and the Far East. It is not so simple with the 168pin DIMM.

Problems with initial SDRAM DIMM designs led to the introduction of the PC100 standard.

Cutting corners on DIMM design and manufacture may result in a working module but under load such DIMMs may fail. Worse failures may manifest themselves only running some software, or when new add-in cards are installed causing extra heat and / or power supply voltages to change.

A nightmare for PC System Assemblers expected to give after sales service and even worse for the end user who cannot fix a problem that comes from a new area – memory performance. Simply put assemblers and users have become used to taking memory for granted.



PC100 – What is it exactly?

It is not an Intel approval in as much as Intel do not test vendors DRAM modules and ‘approve them’. Intel PC100 compliance is also not an Intel endorsement (much as many vendors would like to claim). In the months to follow the launch of the Intel new 100MHz chipset many low cost third party module vendors will claim PC100 compliance and may, intentionally or not, mislead customers.

Intel have published a set of standards that they wish DRAM manufacturers and module manufacturers to follow. These standards make up the PC100 specification. They are;

Standard		Revision
DRAM device standard	Defines the minimum performance levels necessary from the DRAM devices.	15.1
DIMM (module) standard	Defines the design including trace lengths, etc	1.0
SPD (program) standard	Defines the program details for the small serial E ² PROM on the DIMM module	12.0a
Gerber (design) Files	2MX8 DRAM based 4MX16 DRAM based 8MX8 DRAM based	Various

These files in Adobe Acrobat[®] format can be downloaded from Intels web site. The Adobe Acrobat Reader needed can be downloaded from <http://www.adobe.com/>.

Most TPSMs (Third Party SIMM/DIMM Manufacturers) will announce Intel PC100 compatible products on the basis that they have followed the specifications available as shown. Readers of this white paper should be aware of the following however.

Simply building the module to the specification shown is not enough. Within the specification are a large number of options. These are covered on page 8, ‘Standards Within Standards’. Furthermore it is the testing of the modules which is critical.

Most motherboard vendors, including Intel for example, issue a list of approved memory products to work with their motherboards. For the better quality motherboard manufacturers such as Tyan, Intel, Asustek and Elite (ECS) and so on these tests can be quite stringent.

Vanguard PC100 modules will appear on the web pages of the most popular motherboard manufacturers as an approved DIMM supplier.

Summary So Far

Intel PC100 compliant built DIMMs are not the same as a motherboard manufacturers PC100 tested DIMMs, as will appear on most motherboard vendors web sites when the new 100MHz chipsets are launched.



PC100 Features and Benefits – Implementation Issues

The most obvious benefit of the PC100 standard is the knowledge that a PC100 module will work in a 100MHz system clock motherboard. If there are faults with the system it can be safely assumed that the problem doesn't lie with the DIMMs.

The following specification issues exist with manufacturing PC100 DIMMs. NB : 'trace' means the 'wire' connecting the components within the PCB (Printed Circuit Board).

1. Trace Length

Feature	Benefit
The specification calls for matched signal delays for each of the seven signal types:- data, address, 5 x control. Minimum lengths are specified as well as maximums.	Previously only maximum lengths were specified and these were often ignored. PC100 makes these lengths mandatory. Result : better reliability.

2. Trace Width, Spacing

Feature	Benefit
Specifies exact width of the trace lines ('wires') and the space between them.	Controls the impedance and electrical interference (cross talk) making the DIMM more reliable.

3. PCB Specification

Feature	Benefit
The spec calls for 6 layers, and unbroken power and ground connections between the layers.	This gives improved power distribution, better signal integrity and less interference from 'noise' on the circuit. This results in better performance.

4. PCB Layer Gap 'Thickness'

Feature	Benefit
The spec calls for 6 layers, and unbroken power and ground connections between the layers.	This gives improved power distribution, better signal integrity and less interference from 'noise' on the circuit. This results in better performance.

5. Precision matched trace lengths, routing, loading and termination.

Feature	Benefit
For the first time EXACT details are given on all of the items listed.	Benefits include reduced clock reflections and precise signal arrival times between multiple modules. Mix and matching different manufactured DIMMs will be less of a concern so long as they are all PC100 parts.

6. Termination resistors on data lines.

Feature	Benefit
A 'hall mark' of the PC100 DIMM is the neat line of SMT resistors. These are used to reduce 'reflections' on the data interface. Some broker DIMM builders avoid the cost of these but PC100 makes them mandatory.	Data interference from these 'reflections' can cause a '0' to be read as '1'. This is avoided by using 10 Ohm damping resistors.



7. Detailed DRAM device minimum performance criteria.

Feature	Benefit
<p>PC100 DIMMs must be built with PC100 DRAM. It IS possible to build a DIMM with standard DRAM, tweak the SPD program and run the module at 100MHz. We are SURE that many brokers will do this. The PC100 spec however makes PC100 DRAM devices mandatory. For example the DRAM must have a ^tAc of 6nS.</p>	<p>Vanguard has developed a range of die revision DRAMs to pass the PC100 spec. They are referred to as -8H, -8L, etc. Other DRAM vendors have had to do the same to meet the tough requirements of PC100.</p>

8. The SPD (Serial Presence Detect) 2K E²PROM

Feature	Benefit
<p>A PC100 DIMM module contains a 2048 bit serial E²PROM. This contains data programmed by the DIMM manufacturer that identifies the module type and various SDRAM organisation and timing parameters. Some vendors like Atmel have produced special variants of this device such as the 34C042.</p>	<p>This program also contains data on the make, manufacture, date, batch code and serial number for each DIMM. A valuable way to trace and monitor ownership, reliability and so on. In addition the SPD program can 'tweak' the DIMM performance and ensure higher reliability be fine tuning the DRAM access.</p>



Standards Within Standards – BIOS Variations, SPD Programs, etc.

At the time of writing this version 1.0a of the white paper it is apparent that many, many DRAM manufacturers and TPSMs are having the most extra ordinary difficulty with the PC100 DIMM tests. Variations between vendors in the programming of the SPD are causing issues as are the very tight manufacturing constraints.

As a result some vendors are allegedly launching a new 100MHz based motherboard with an Award BIOS that will not interface or use the SPD program on the PC100 DIMM. Whilst this will undoubtedly result in down grade for system performance it will allow a far wider range of synchronous DIMMs to be used with the board. Time will tell whether end users and the PC press will insist on such boards becoming fully PC100 compatible.

Programming the SPD

The non volatile serial E²PROM, such as the Atmel AT24C02, is used to store the information shown in the table taken from Intels SPD Specification 1.2A, publicly available from the internet. However it can be seen that there is a large amount of 'spare' memory on the device used for optional items.

Many 'cheaper' manufacturers are ignoring these options.

Many customers and system assemblers may find however that there are a number of advantages in sourcing DIMMs that have been programmed with the manufacturers make, model number and serial number. In addition many larger customers may be able to negotiate having the SPD programmed with their name, make and model number during module production and test.

Benefits in such programming.

1. Traceability	Via the use of a simple utility it will be possible for the system assembler to interrogate a users PC to establish the make, model and serial number – or not, of the memory being used.
2. System Failure	Identifying unknown, or unapproved DIMMs which may be responsible for system failure or unreliability will for the first time be possible.
3. Theft, Fraud	The serial number CAN BE reprogrammed unless a 'Permanent Write Protect' E ² PROM is used (see next heading). However faulty re-programming will damage the DIMM making it useless or unreliable. The SPD needs programming by a skilled technician. Therefore the SPD will enable some traceability for theft or fraud.
4. Return Goods	Returning parts will be easier since faulty items will be more easily identified.
5. Branding	It should be possible for BIOS vendors to access the SPD during POST to identify the make of the module during the memory count making branding of the memory possible for the first time.
6. Upgrades	The user will be able to simply identify his / her existing memory making matching memory for upgrades a much more simple exercise.

Next page – SPD Program Details.



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PC SDRAM Serial Presence Detect (SPD) Specification Dec, 1997 11 of 28 Revision 1.2A

4.0 Serial Presence Detect EEPROM Data

Table 5: Serial Presence Detect Data Format

Byte Number Function Required / Optional

0	Defines # of bytes written into serial memory at module manufacturer	Required
1	Total # of bytes of SPD memory device	Required
2	Fundamental memory type (FPM, EDO, SDRAM..) from Appendix A	Required
3	# of row addresses on this assembly (includes Mixed-size Row addr)	Required
4	# Column Addresses on this assembly (includes Mixed-size Col addr)	Required
5	# Module Rows on this assembly	Required
6	Data Width of this assembly	Required
7	.. Data Width continuation	Required
8	Voltage interface standard of this assembly	Required
9	SDRAM Cycle time , CL=X (highest CAS latency)	Required
10	SDRAM Access from Clock (highest CAS latency)	Required
11	DIMM Configuration type (non-parity, ECC)	Required
12	Refresh Rate/Type	Required
13	Primary SDRAM Width	Required
14	Error Checking SDRAM width	Required
15	Minimum Clock Delay Back to Back Random Column Address	Required*
16	Burst Lengths Supported	Required*
17	# of Banks on Each SDRAM Device	Required*
18	CAS# Latencies Supported	Required*
19	CS# Latency	Required*
20	Write Latency	Required*
21	SDRAM Module Attributes	Required*
22	SDRAM Device Attributes: General	Required*
23	Min SDRAM Cycle time at CL X-1 (2nd highest CAS latency)	Required*
24	SDRAM Access from Clock at CL X-1 (2nd highest CAS latency)	Required*
25	Min SDRAM Cycle time at CL X-2 (3rd highest CAS latency)	Optional*
26	Max SDRAM Access from Clock at CL X-2 (3rd highest CAS latency)	Optional*
27	Min Row Precharge Time (Trp)	Required*
28	Min Row Active to Row Active (Trrd)	Required*
29	Min RAS to CAS Delay (Trcd)	Required*
30	Minimum RAS Pulse Width (Tras)	Required*
31	Density of each row on module (mixed, non-mixed sizes)	Required
32-61	Superset Information (may be used in future)	
62	SPD Data Revision Code	Required
63	Checksum for bytes 0-62	Required
64-71	Manufacturer's JEDEC ID code per JEP-108E	Optional
72	Manufacturing Location	Optional
73-90	Manufacturer's Part Number	Optional
91-92	Revision Code	Optional
93-94	Manufacturing Date	Optional
95-98	Assembly Serial Number	Optional
99-125	Manufacturer Specific Data	Optional
126	Intel specification frequency	Required
127	Intel Specification CAS# Latency support	Required
128+	Unused storage locations	

Notes: **Required/Optional*** (bold*) are SDRAM only bytes

For full details of the SPD programming specification please see Intels web page to download the latest version at: <http://developer.intel.com/design/pcisets/memory/index.htm>



SPD and ‘Permanent Write protect’

The author is aware of at least two makes of serial E²PROM for which the lower half of the device incorporates a software write protection feature while hardware write protection for the entire device array is available via an external pin as well. This would enable a manufacturers details to be permanently entered onto the SPD making fraud even more difficult.

Atmel make a device – the AT34C02 which does this. A data sheet can be downloaded from the following URL: <http://www.atmel.com/atmel/products/prod162.htm>

Catalyst also make a similar device – the CAT34WC02 available in either TSSOP or SOIC.

DIMM Options

PC100 synchronous DIMMs are available in the following configurations;

SIZE (Mbytes)	Organisation	DRAM Used	DRAM Org.	# of DRAMs
16Mbyte	2MX64 single sided	16Mbit	2MX8	8
32Mbyte	4MX64 double sided	16Mbit	2MX8	16
32Mbyte	4MX64 single sided	64Mbit	4MX16	4
64Mbyte	8MX64 single sided	64Mbit	8MX8	8
64Mbyte	8MX64 single sided	64Mbit	4MX16	8
64Mbyte	8MX64 single sided	128Mbit	8MX16	4
128Mbyte	16MX64 double sided	64Mbit	8MX8	16
128Mbyte	16MX64 single sided	128Mbit	8MX16	8
128Mbyte	16MX64 single sided	128Mbit	16MX8	8
256Mbyte	32MX64 double sided	128Mbit	16MX8	16
256Mbyte	32MX64 single sided	256Mbit	16MX16	8
512Mbyte	64MX64 double sided	256Mbit	16MX16	16



DIMM Manufacturing

The major reason that PC100 DIMMs will be more expensive than standard DIMM modules is the expense of the equipment necessary to manufacture and test the modules. A simple breakdown can be made as follows, the PCB is more expensive at ~\$5 than the average 72 pin SIMM PCB at ~\$1.50; the pick and place, silk screen and so on is the same but the programming and testing takes longer.



To test DIMMs operating at more than 100MHz however needs specialist test equipment. The Hewlett Packard HP8300 pictured left costs a reputed ~\$1,500,00 each and can test only ONE DIMM at a time!

However this multimedia Model P machine features 200MHz I/O and up to 300MHz clock and can accurately test high speed busses with input/output data rates of up to 400Mbits/s. See: www.tmo.hp.com/tmo/datasheets/English/HP83000MMRev.html

The Advantest T5581 comes in a little cheaper at approximately \$750,000 and can test up to 64 DRAMs (for DIMMs divide by DRAMs per DIMM) simultaneously. The maximum clock rate supported is however 'only' 250MHz. Advantest expect to sell a 100 of these machines in 1998. The T5581 is also smaller than previous machines. See: <http://www.advantest.co.jp/11-23t-e.html>



Some of the TPSM's are working on cheaper alternative test machines. However these have yet to be announced. Undoubtedly we will see the introduction of lower cost, larger volume testers but in the short to medium term the start up or on going cost to manufacture PC100 modules is expensive.

- End -



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